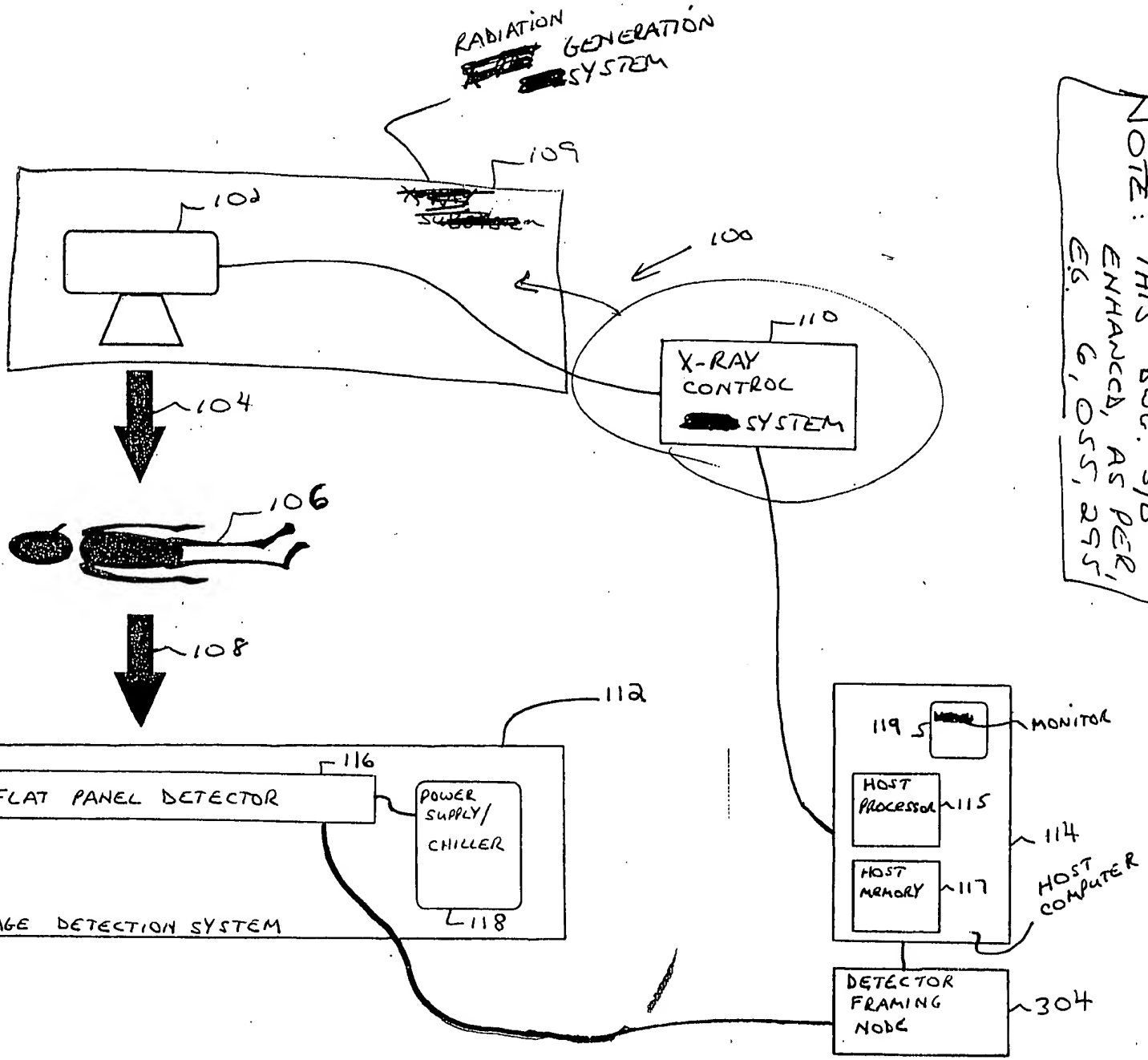
PATENT APPLICATION



NOTE: THIS DWG. S/B ENHANCED, AS PER, E.G. 6,055,295

FIG. 1

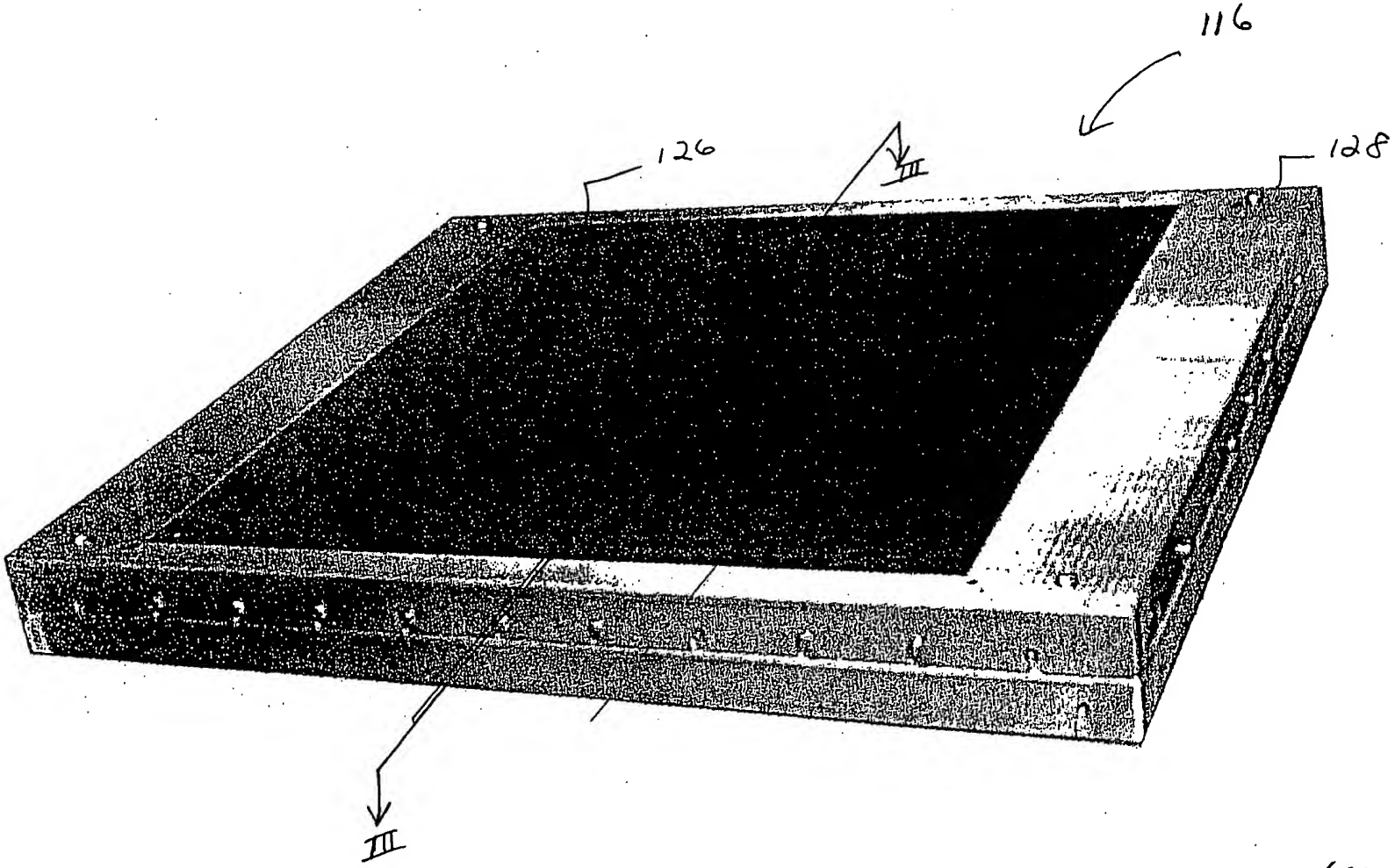


FIG. 2 (PRIOR ART)

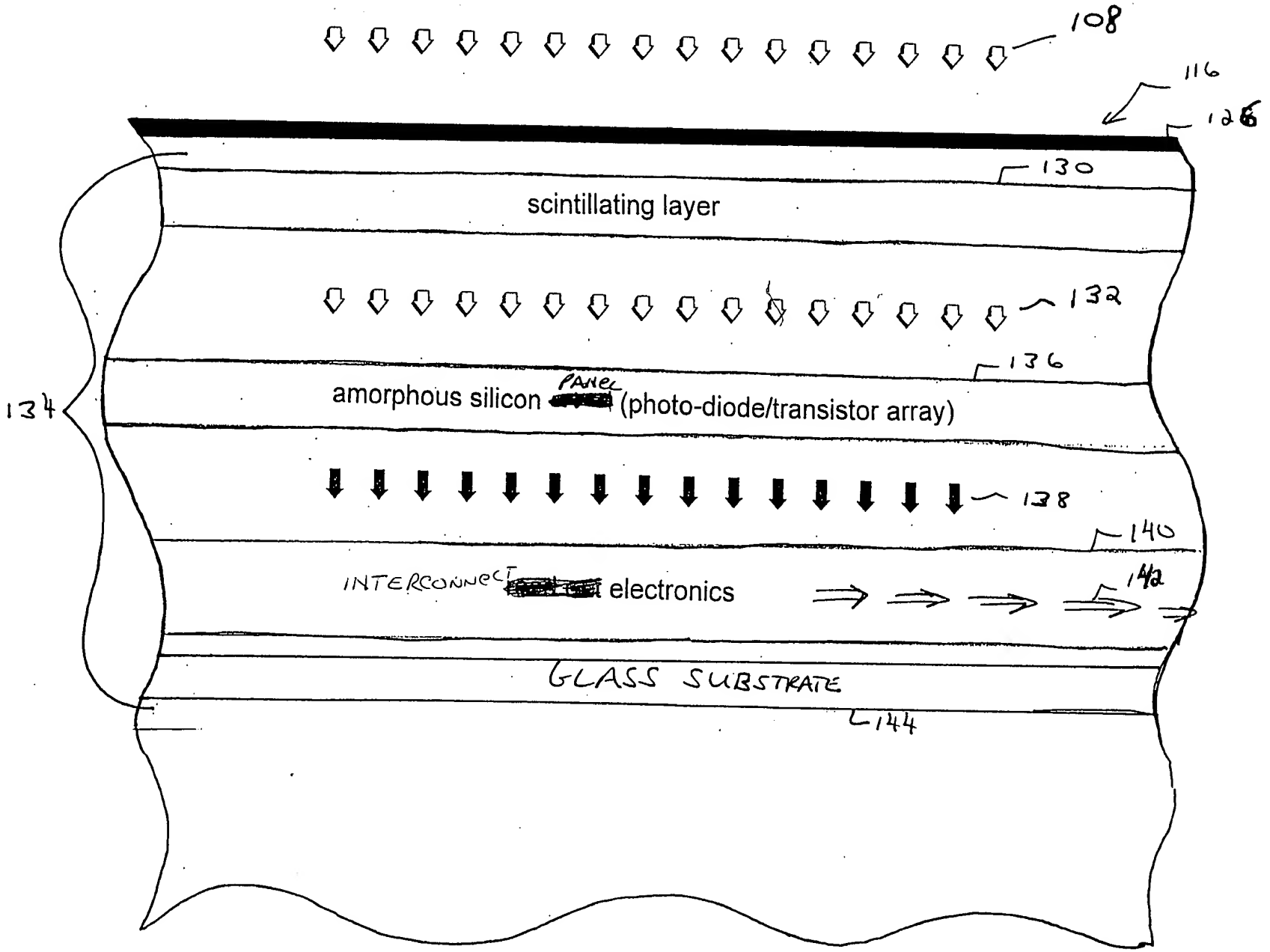

108
116
126
130
scintillating layer
132
136
134
amorphous silicon PANEL (photo-diode/transistor array)
138
140
INTERCONNECT electronics
142
GLASS SUBSTRATE
144

FIG. 3

PATENT Serial #2260

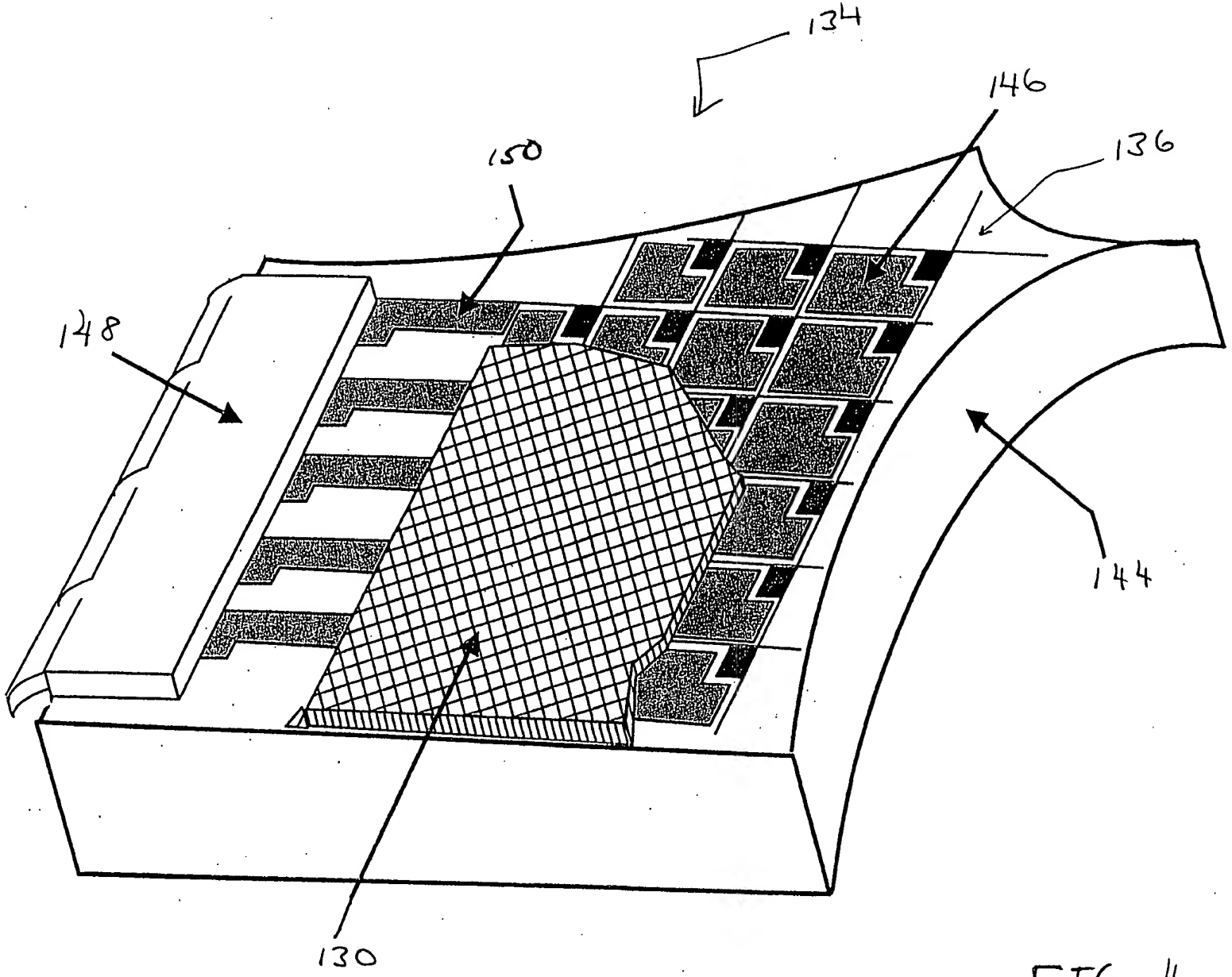


FIG. 4
(PRIOR ART)

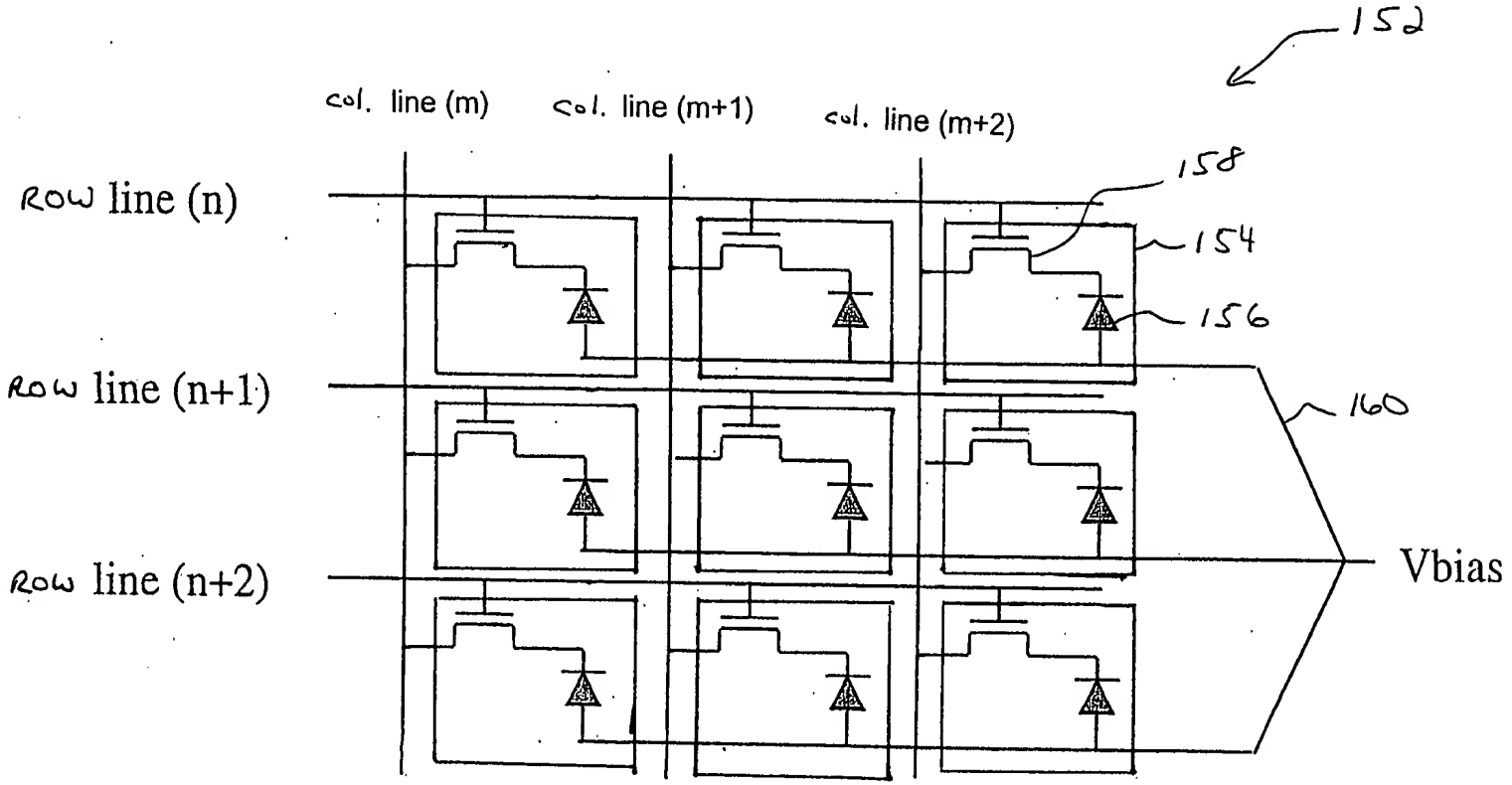


FIG. 5
(PRIOR ART)

TOSCTO-6654/2560

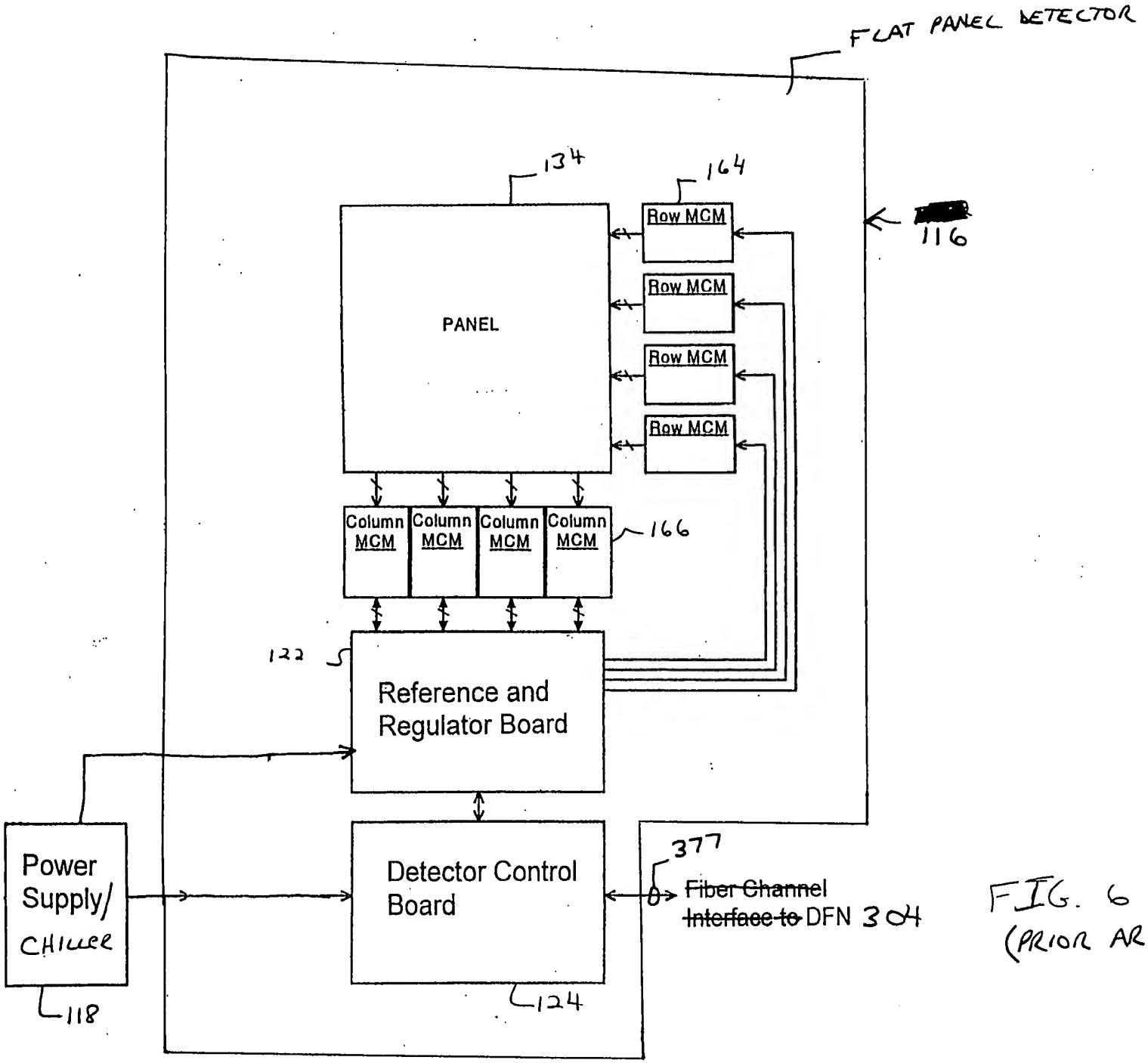


FIG. 6
(PRIOR ART)

PATENT SEARCH

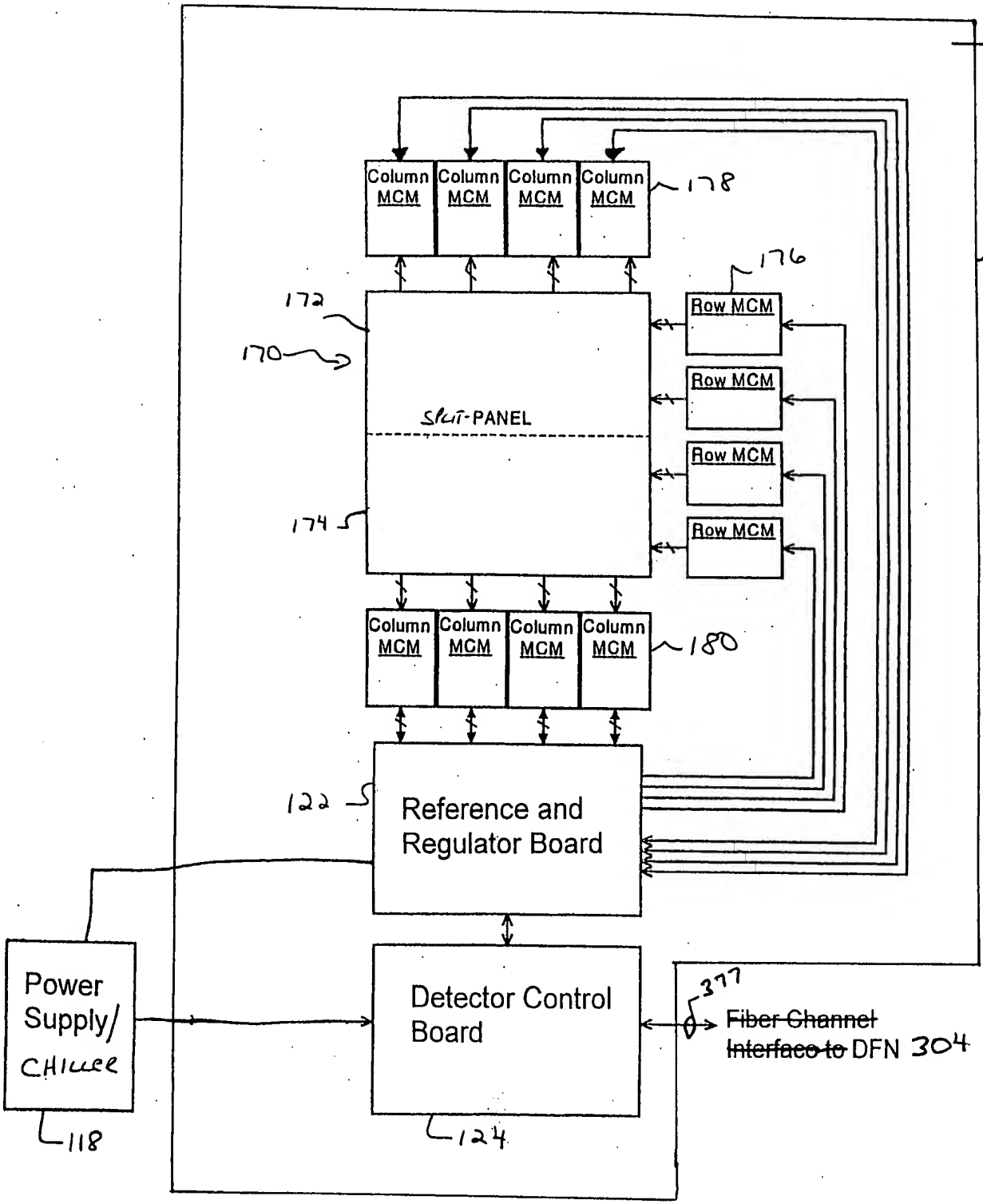
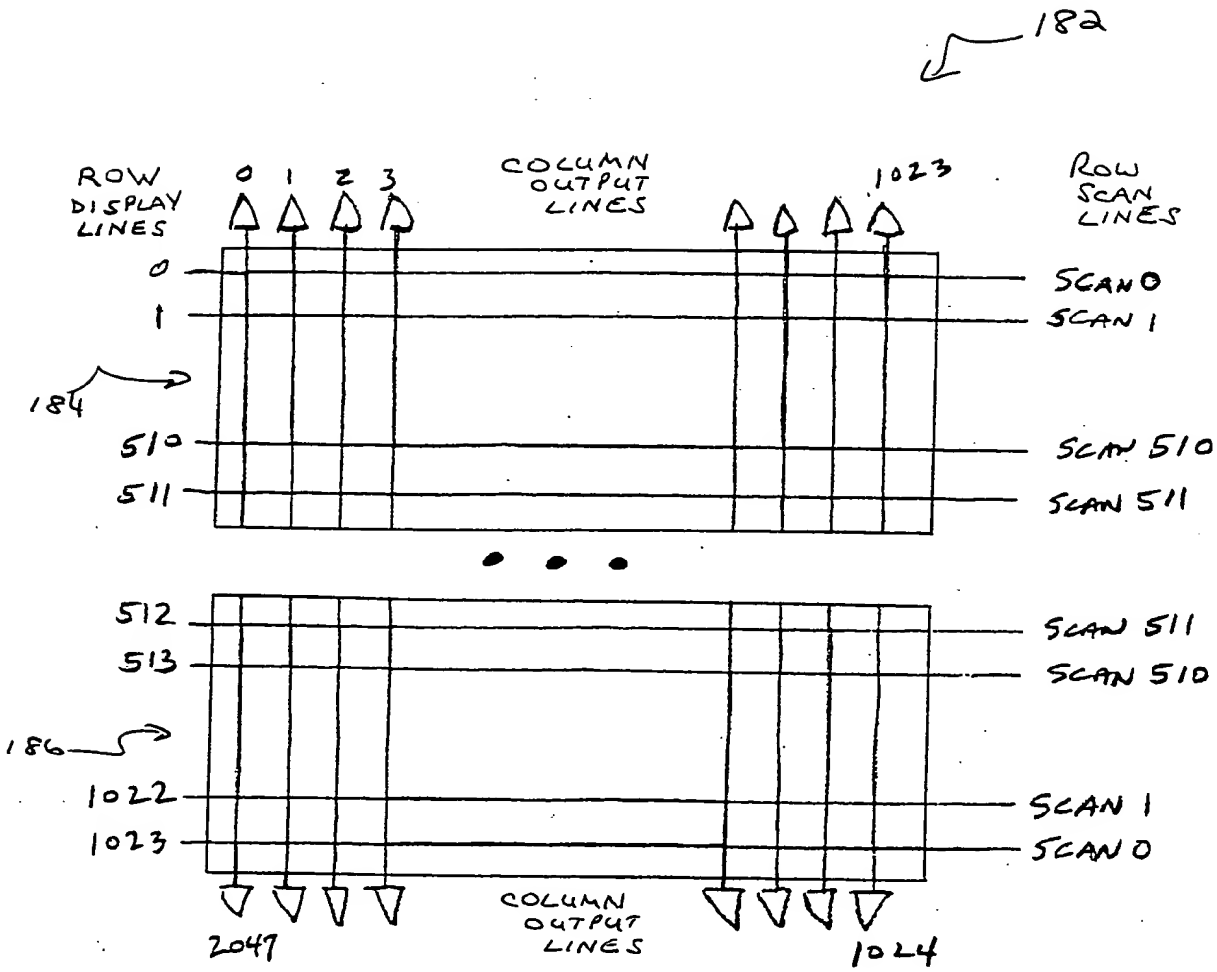


FIG. 7
(PRIOR ART)



CARDIAC/SURGICAL DIGITAL X-RAY PANEL

FIG. 8
(PRIOR ART)

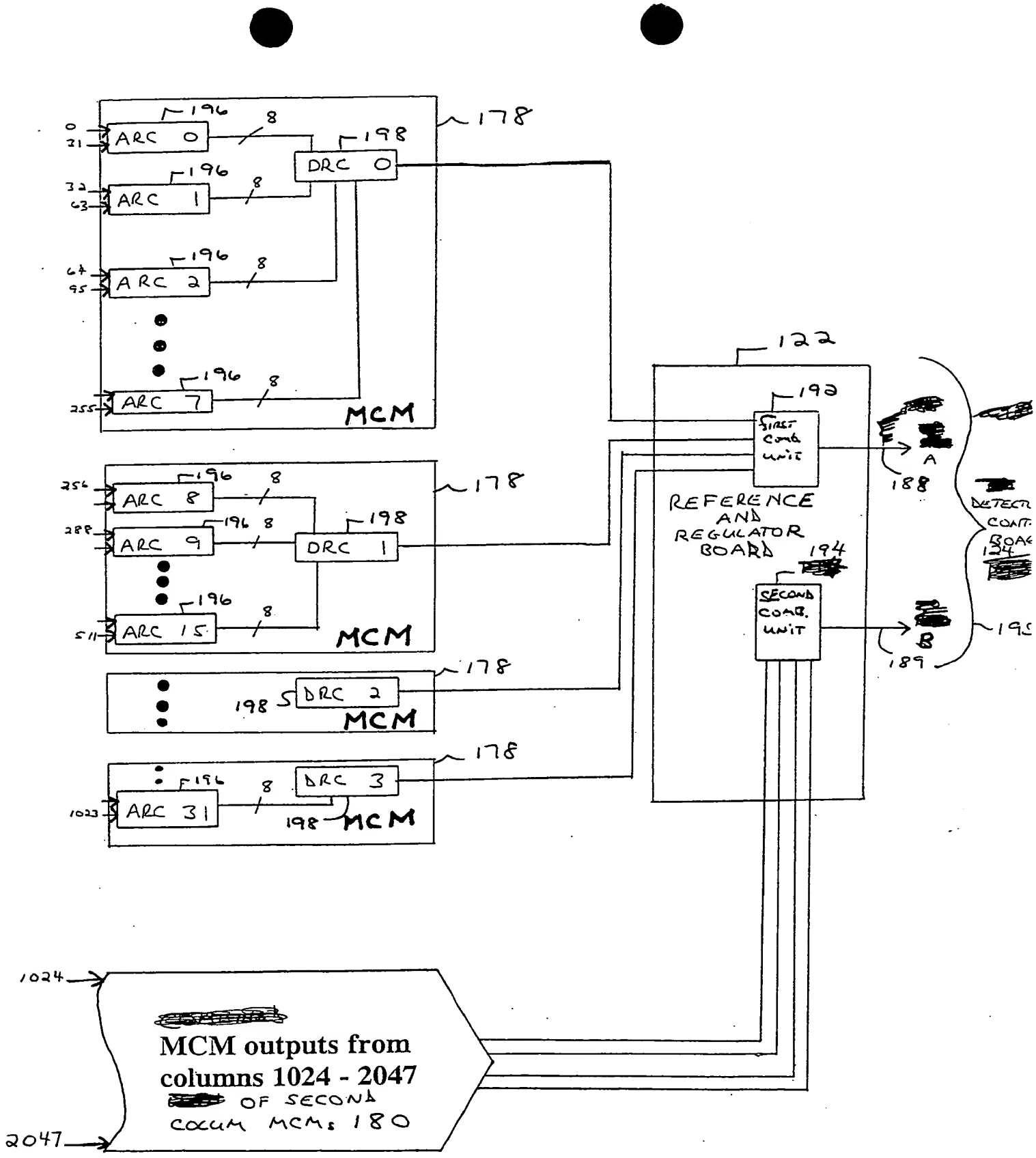


FIG. 9
(PRIOR ART)

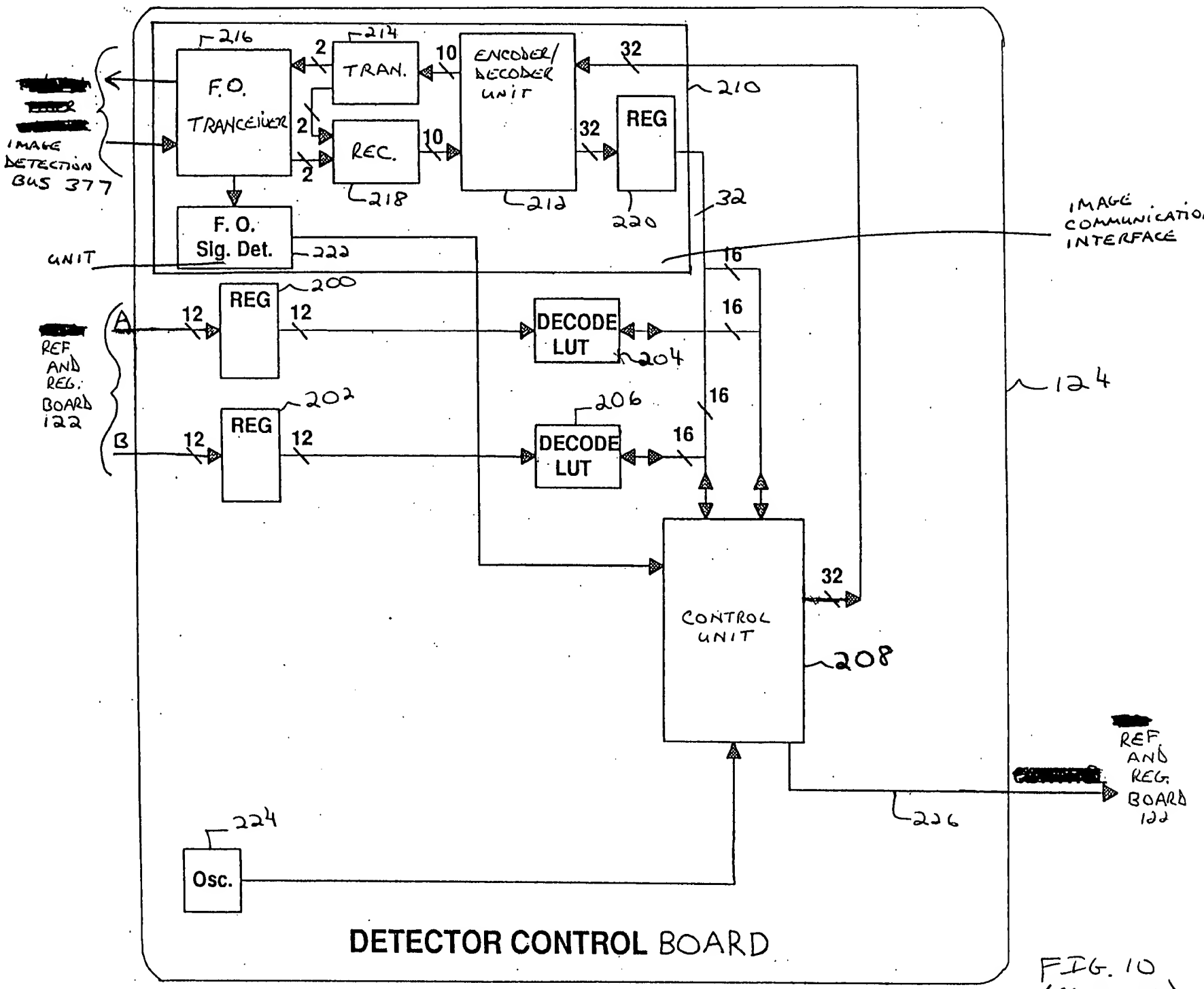
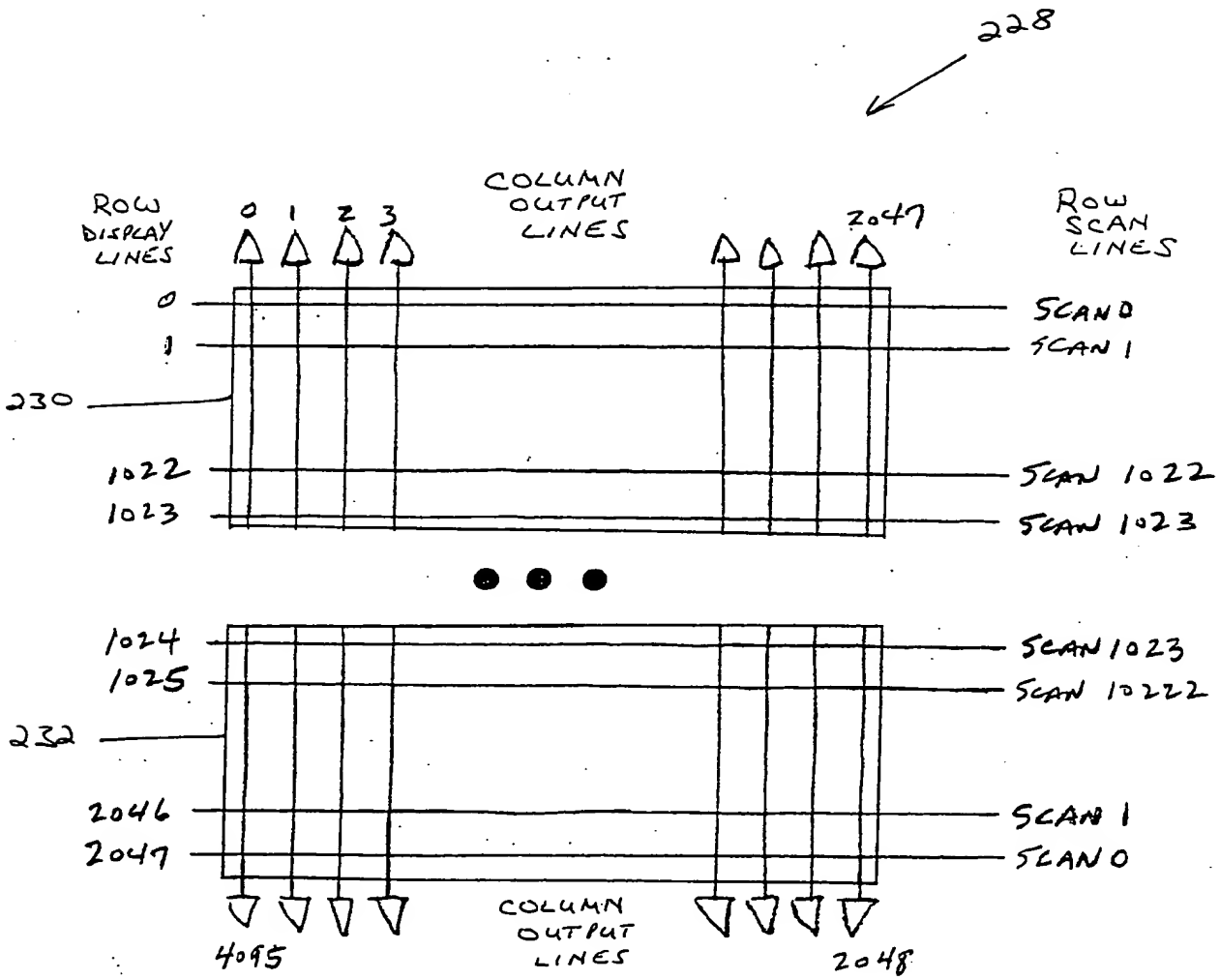


FIG. 10
(PRIOR ART)



RADIOGRAPHY DIGITAL X-RAY PANEL

FIG. 11
(PRIOR ART)

DOCKET SEARCH

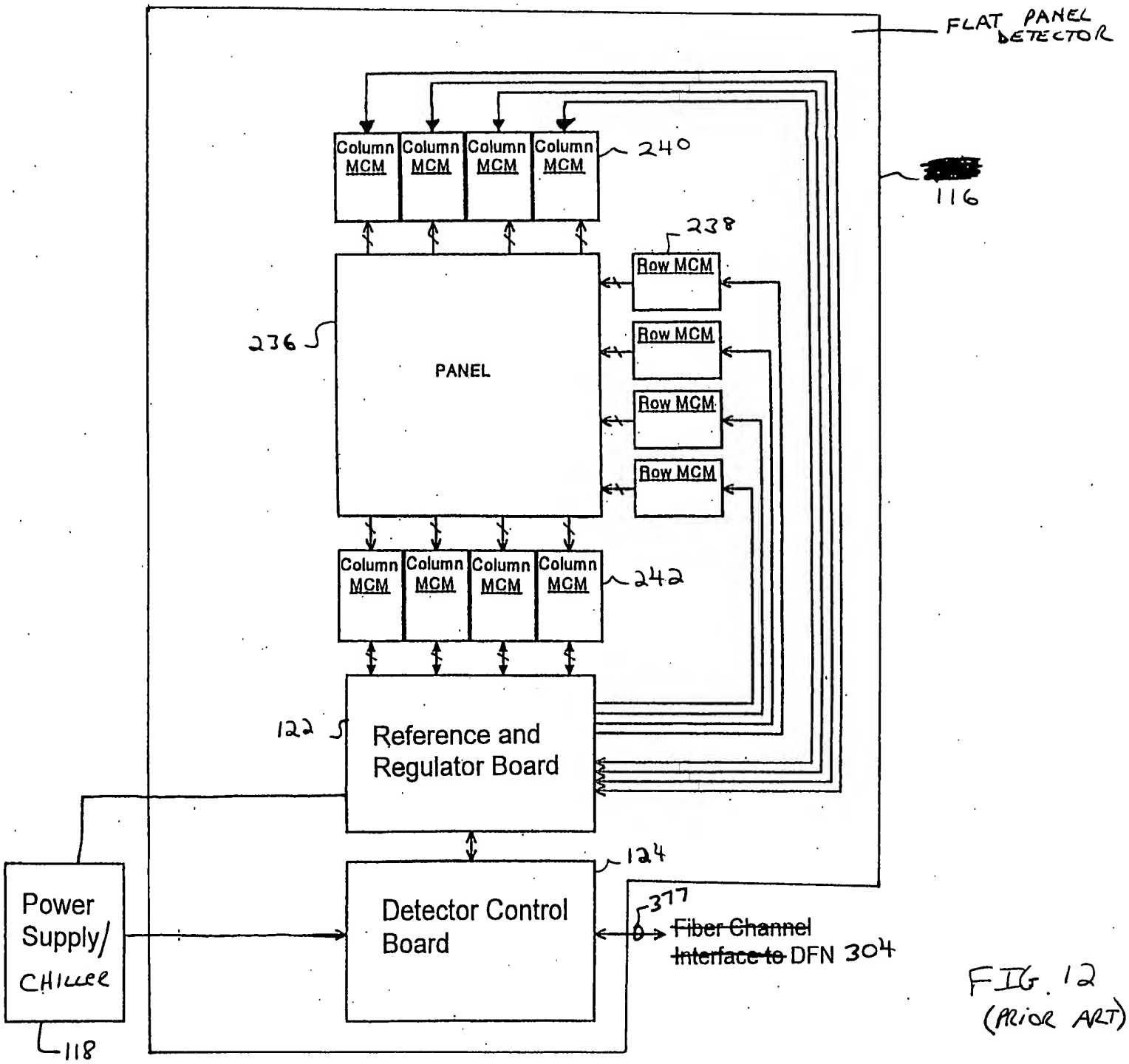
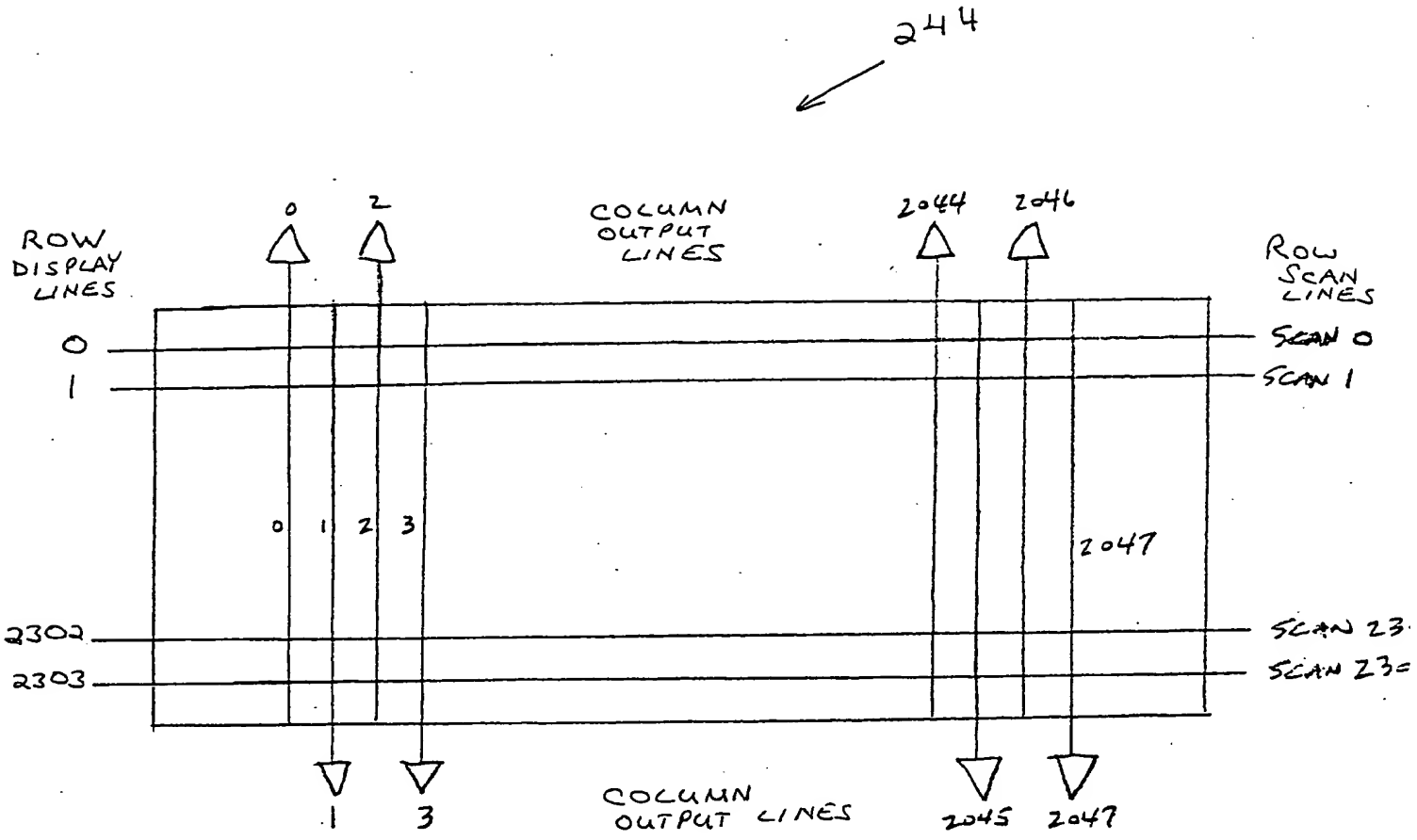


FIG. 12
(PRIOR ART)



MAMOGRAPHY DIGITAL X-RAY PANEL

FIG. 13
(PRIOR ART)

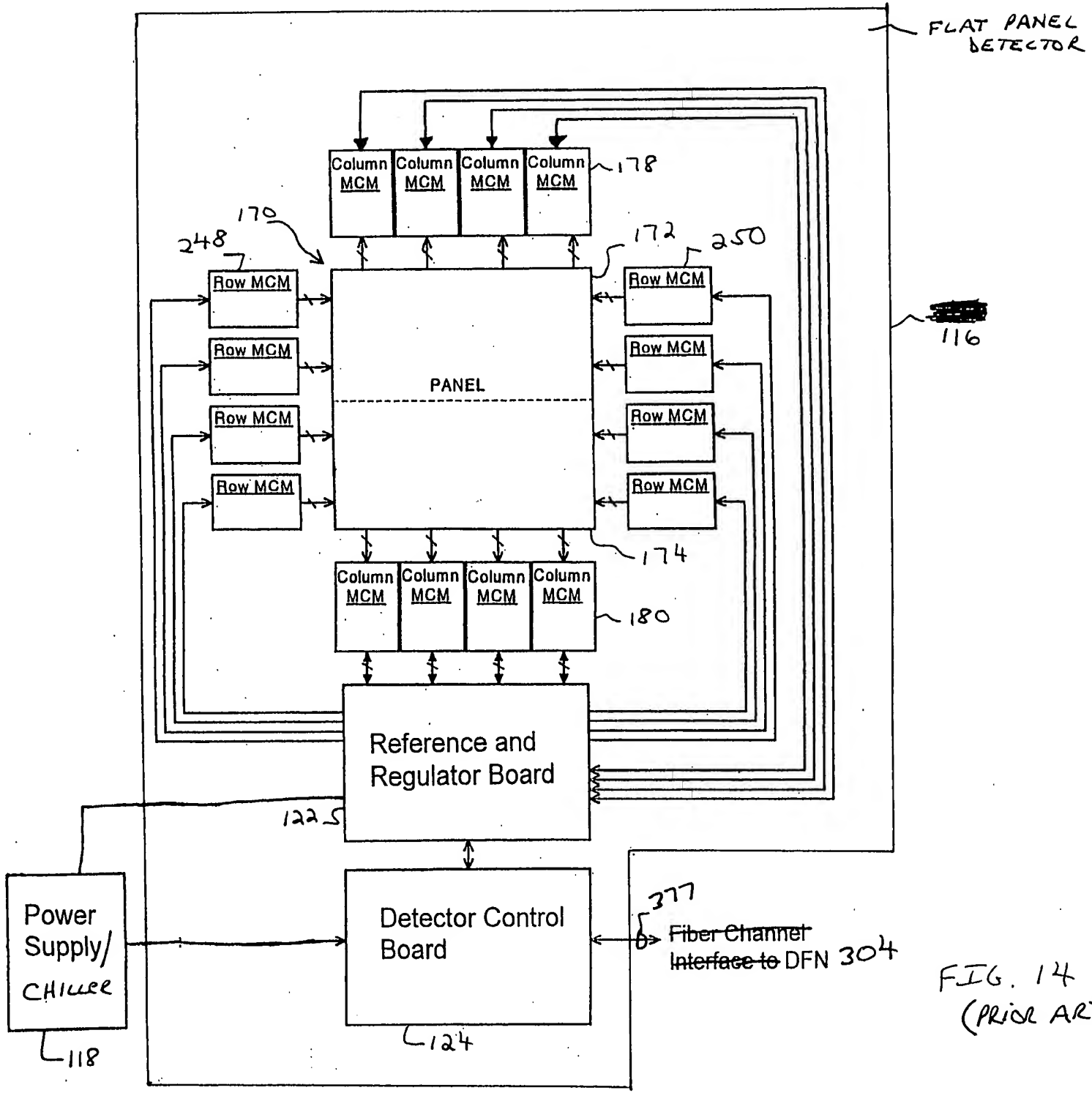


FIG. 14
(PRIOR ART)

\\NTSERVER\WORK\1346\todd-DFN cases\drawing stuff\FIG. 15.doc

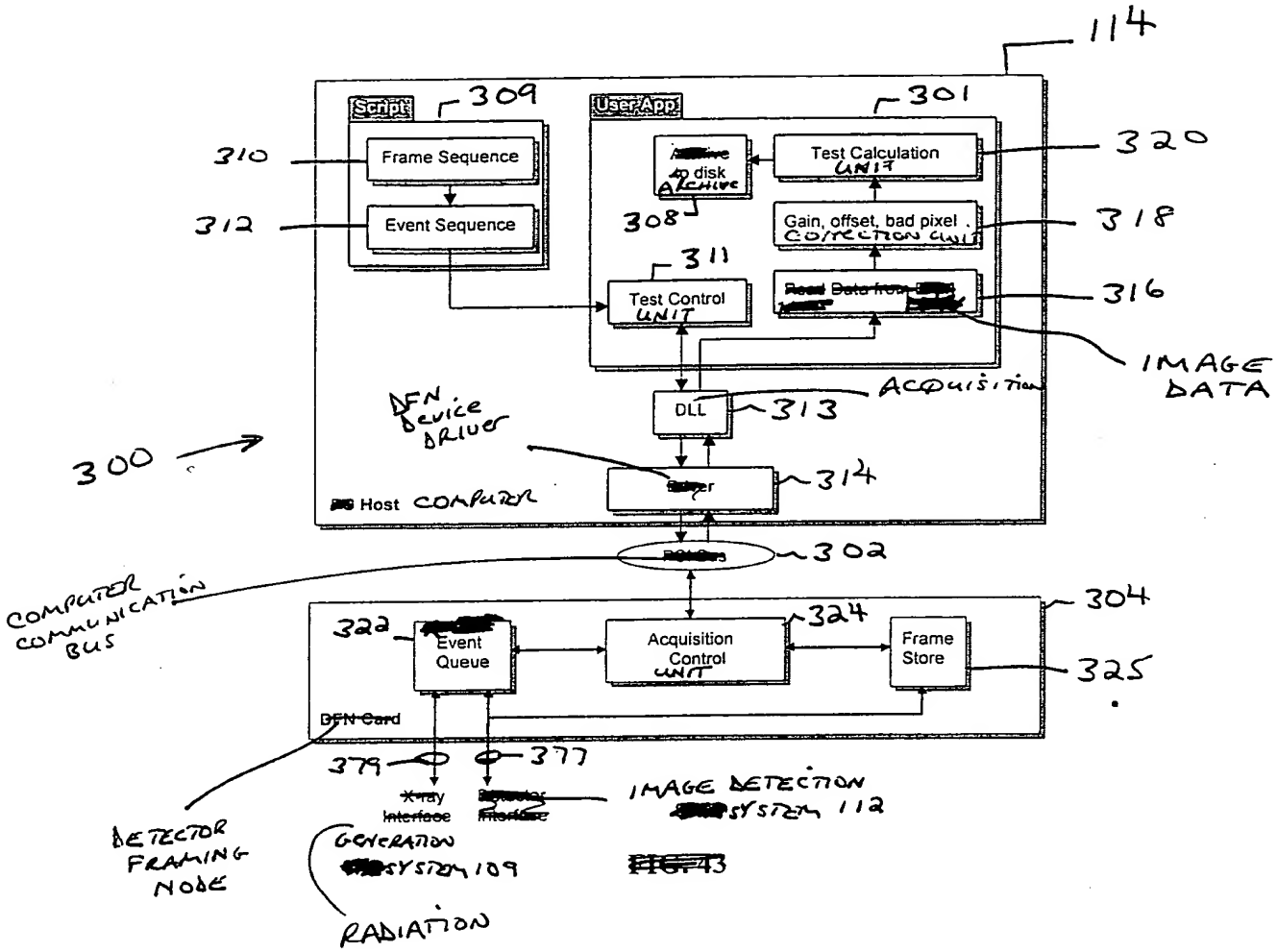


FIG. 15

DOCKET SEARCH

w:\1346\todd-dfn cases\drawings\dwg-01 (page 3)

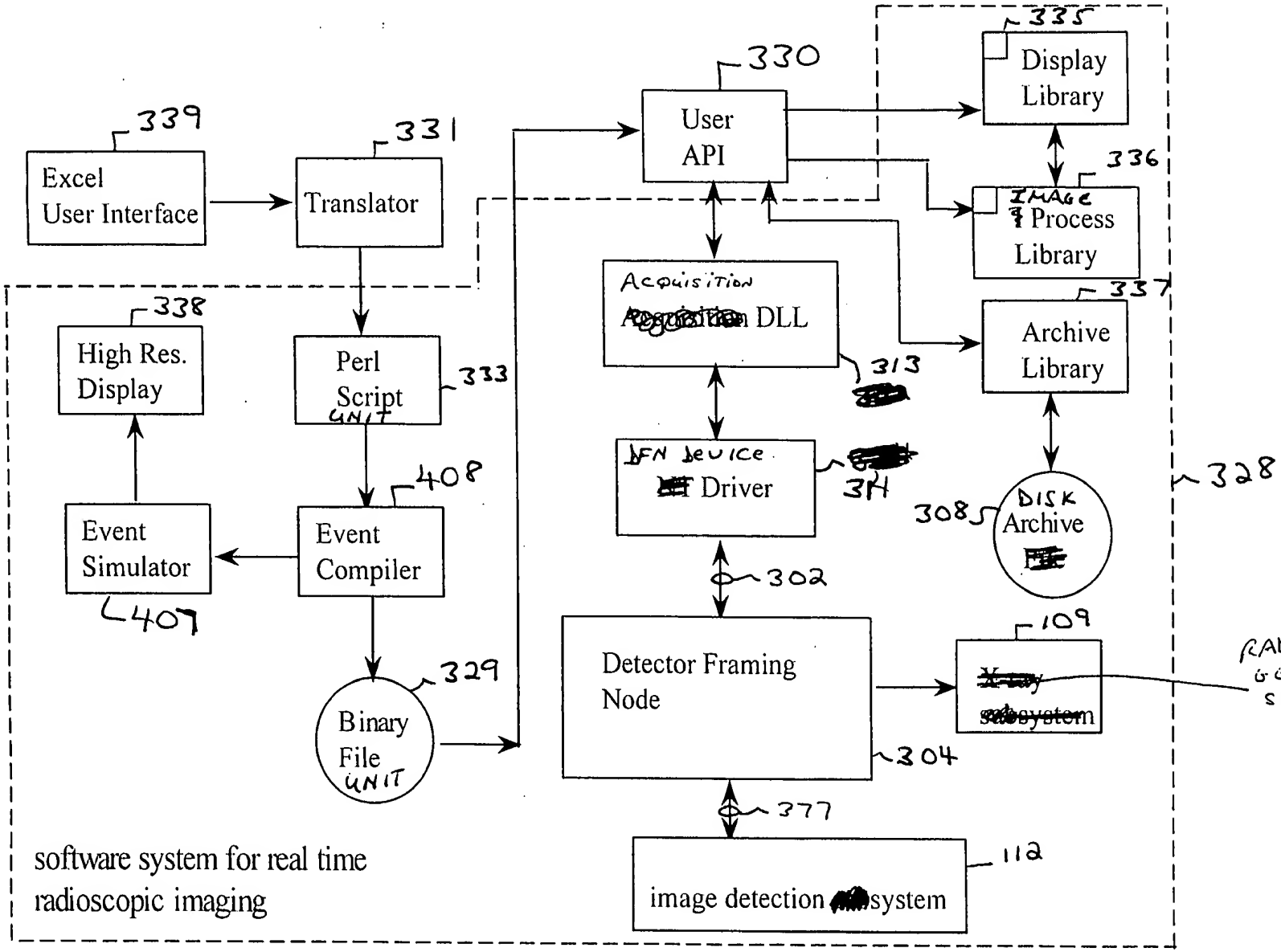
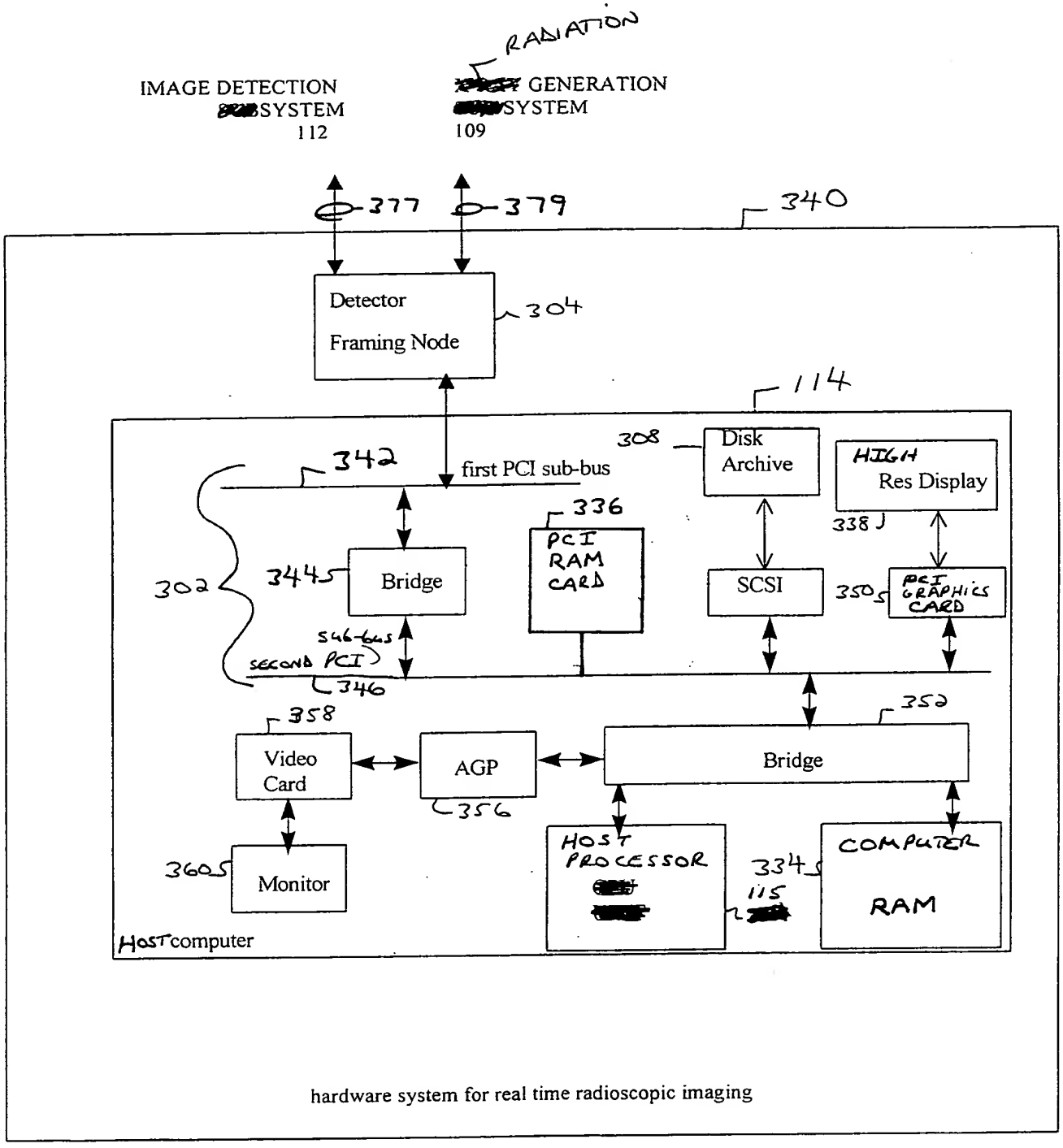


FIG. 16



hardware system for real time radioscopic imaging

FIG. 17

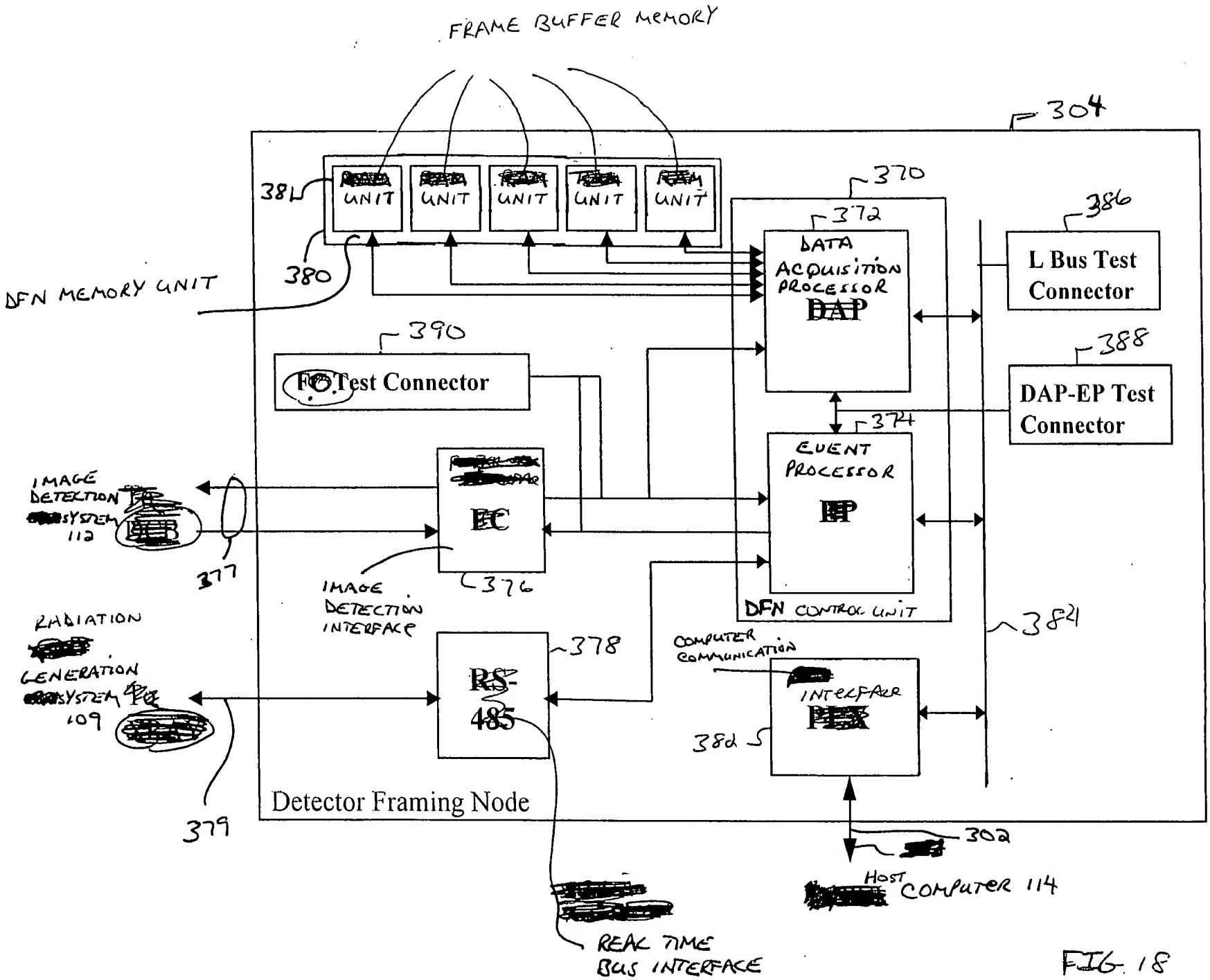

FRAME BUFFER MEMORY
304
381
UNIT
UNIT
UNIT
UNIT
UNIT
380
DFN MEMORY UNIT
370
372
DATA ACQUISITION PROCESSOR
DAP
386
L Bus Test Connector
390
FO Test Connector
388
DAP-EP Test Connector
374
EVENT PROCESSOR
EP
IMAGE DETECTION SYSTEM 112
EC
377
376
IMAGE DETECTION INTERFACE
DFN CONTROL UNIT
384
RADIATION GENERATION SYSTEM 109
378
RS-485
COMPUTER COMMUNICATION INTERFACE
382
379
Detector Framing Node
302
HOST COMPUTER 114
REAL TIME BUS INTERFACE

FIG. 18

		(fm/sec)	length	Latency	memory	offset	gbr
Panel Setup	Real Time	30	unlimited	< 5 frames	host	none	
Single Frame	Post Process	-	-	Delay ~.1 sec	"	y	
Single Frame	Post Process	-	-	Delay ~.2 sec	"	y	y
Real Time	Real Time	R	Unlimited	< 5 frames	host	none	
Real Time	Real Time	R - X	Unlimited	< 5 frames	"	y	
Real Time	Real Time	R - Y	Unlimited	< 5 frames	"	y	y

FIG. 19

Modality	image size	Frames Stored host memory
Cardiac	1024 x 1024	200
Rad	2048 x 2048	50
Mammo	2304 x 2048	44

FIG. 20

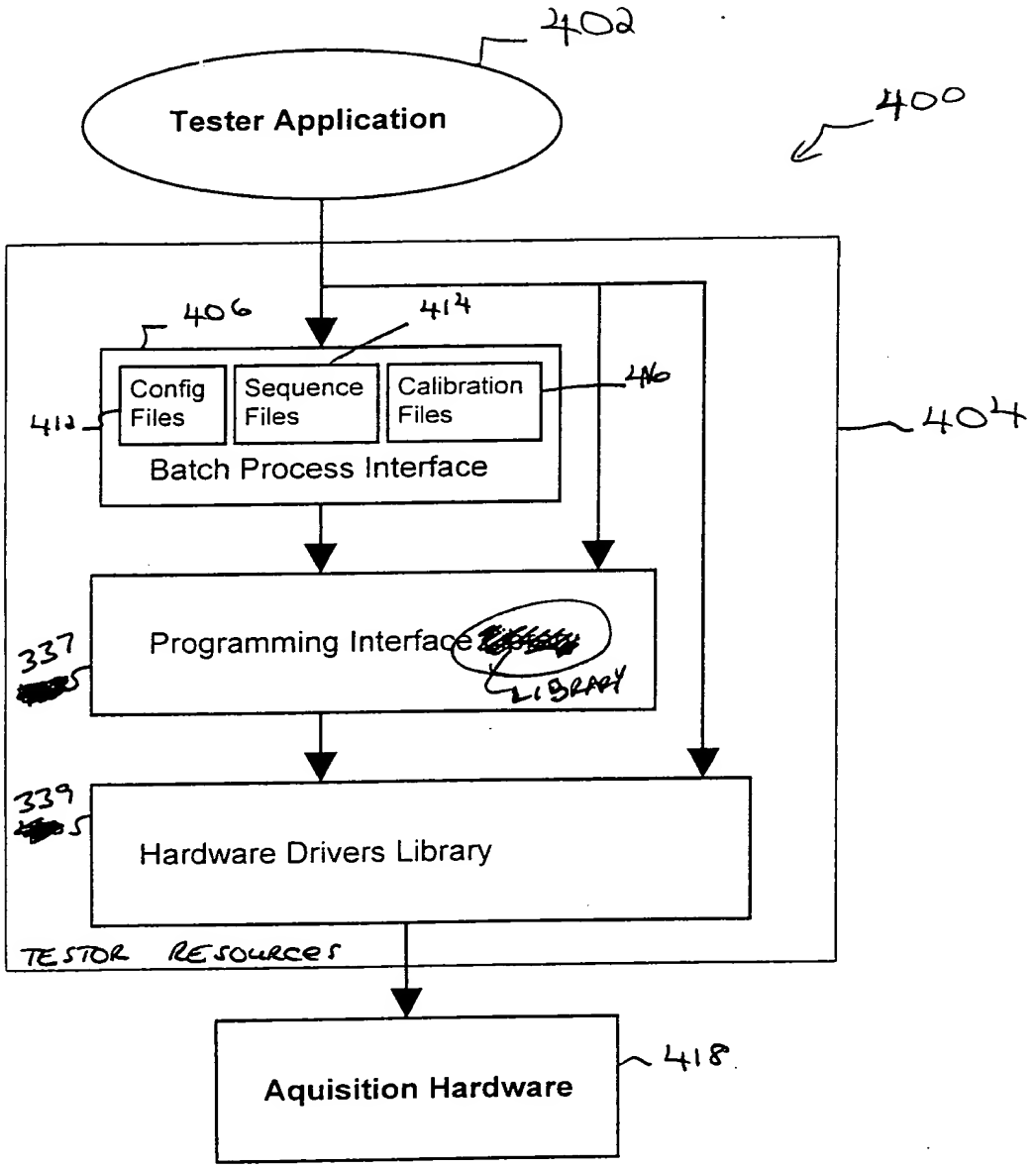

402
Tester Application
400
406
414
Config Files
Sequence Files
Calibration Files
416
412
Batch Process Interface
404
337
Programming Interface
LIBRARY
339
Hardware Drivers Library
TESTOR RESOURCES
418
Aquisition Hardware

FIG. 21

W:\1346\todd-DFN cases\drawings\hardware drivers interface.doc

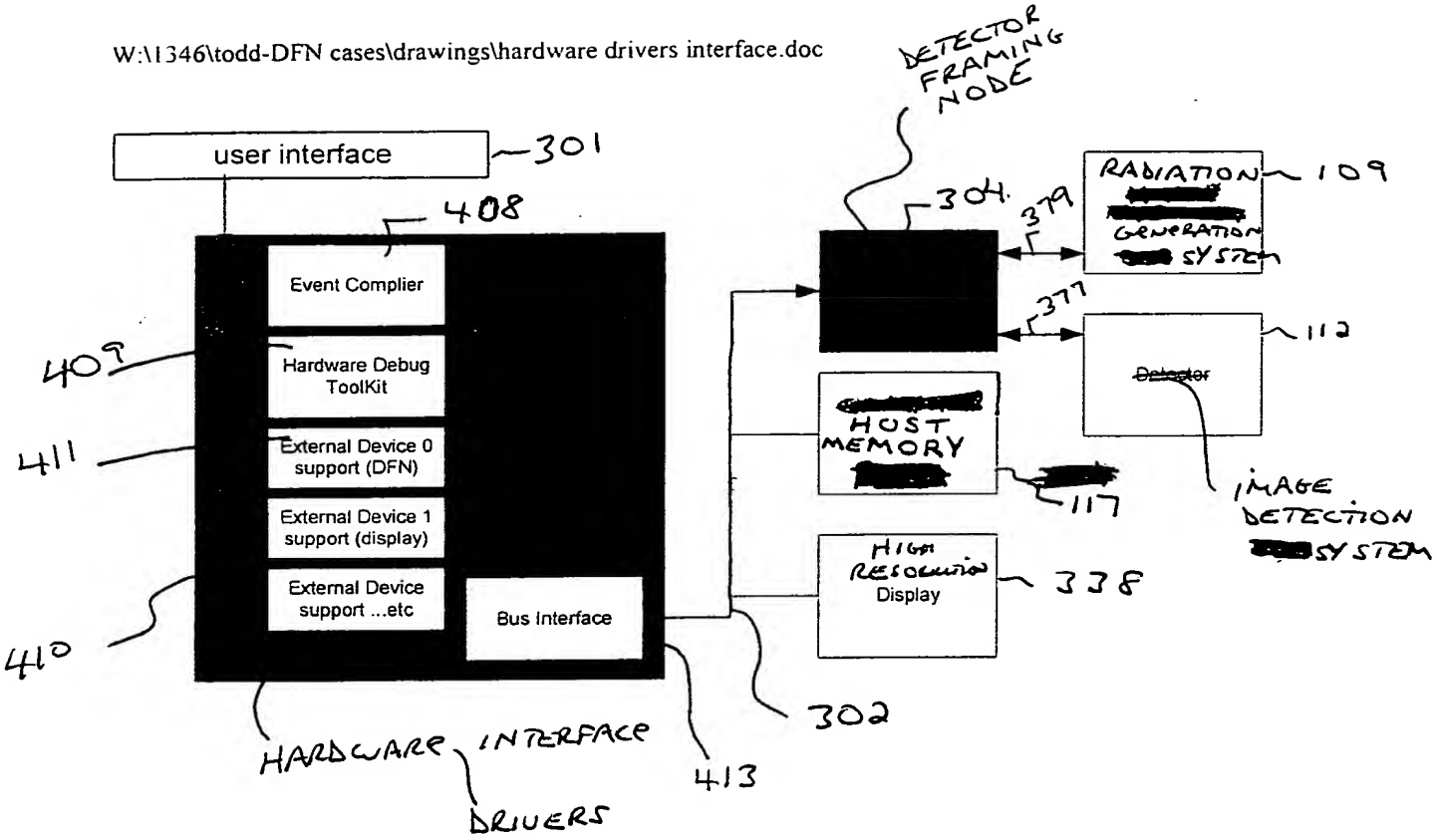


FIG. 22

W:\1346\todd-DFN cases\drawings\detector control board settings.doc

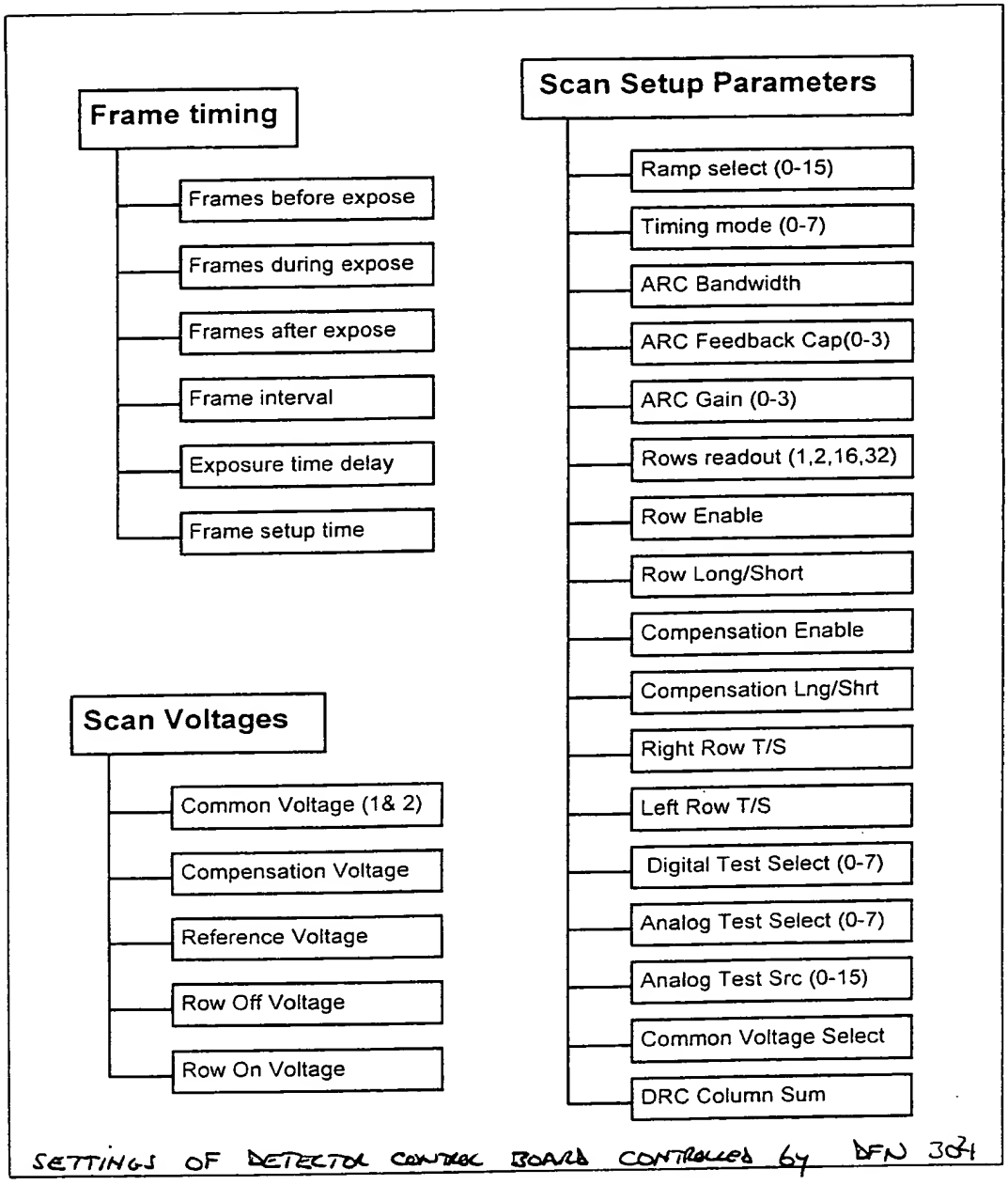


FIG. 23

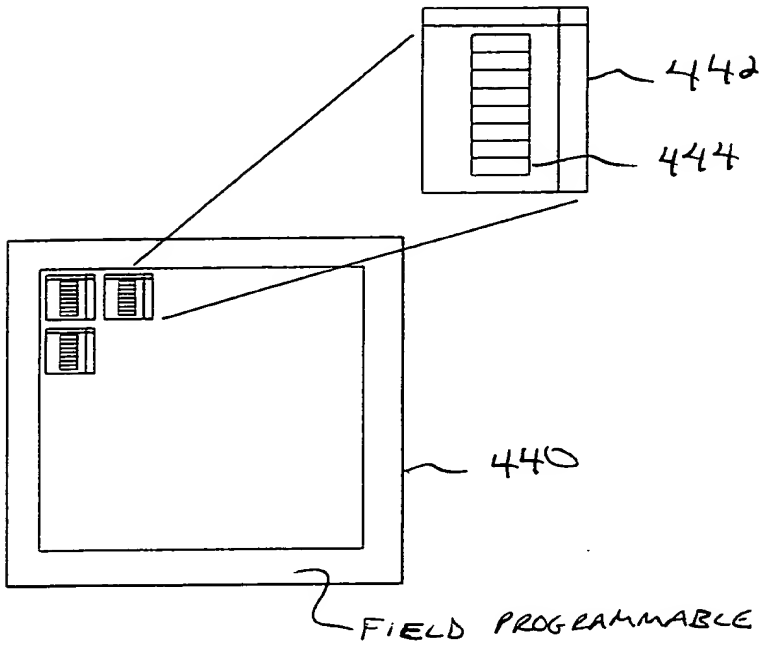


FIG. 24

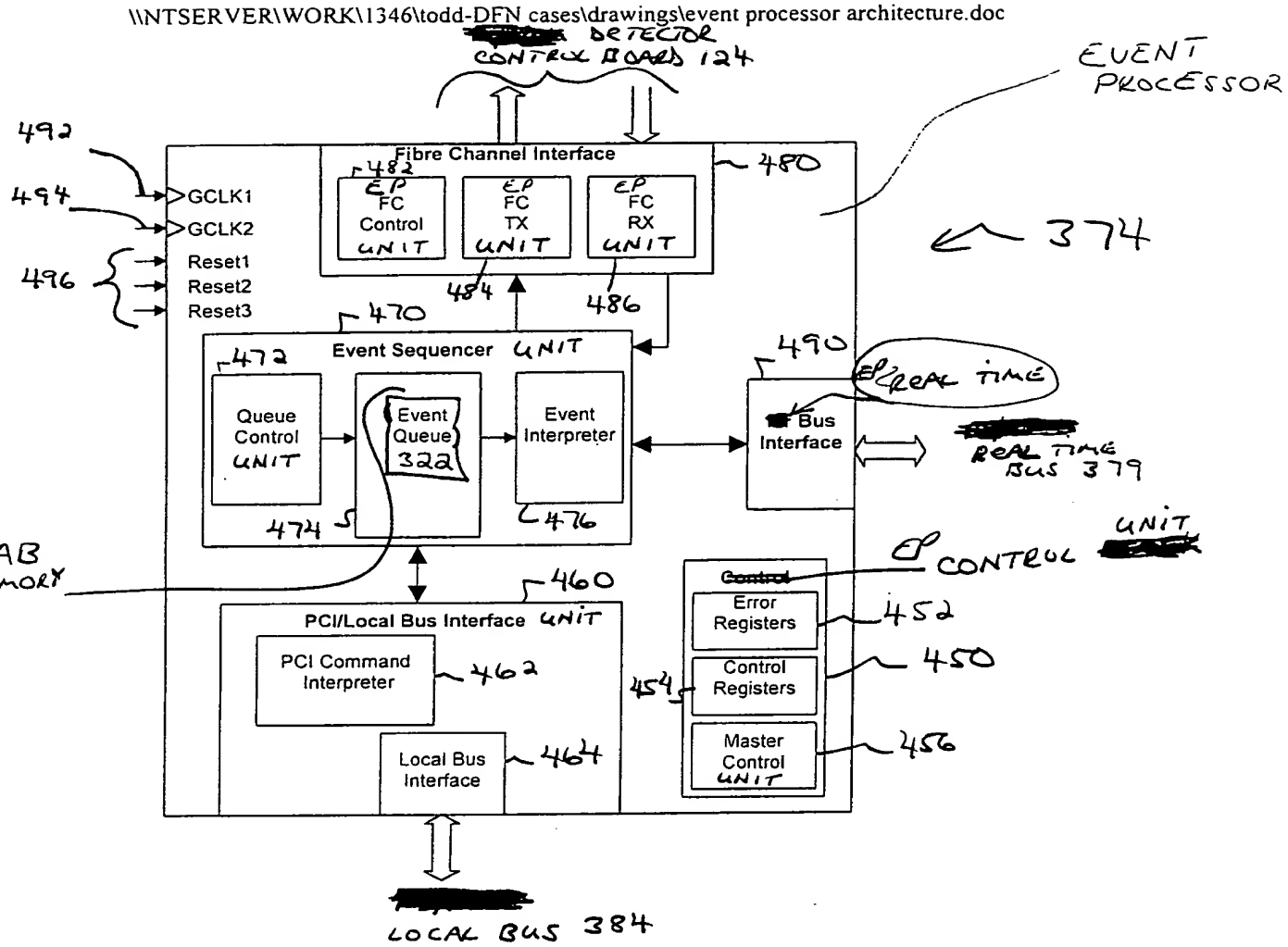


FIG. [redacted] 25

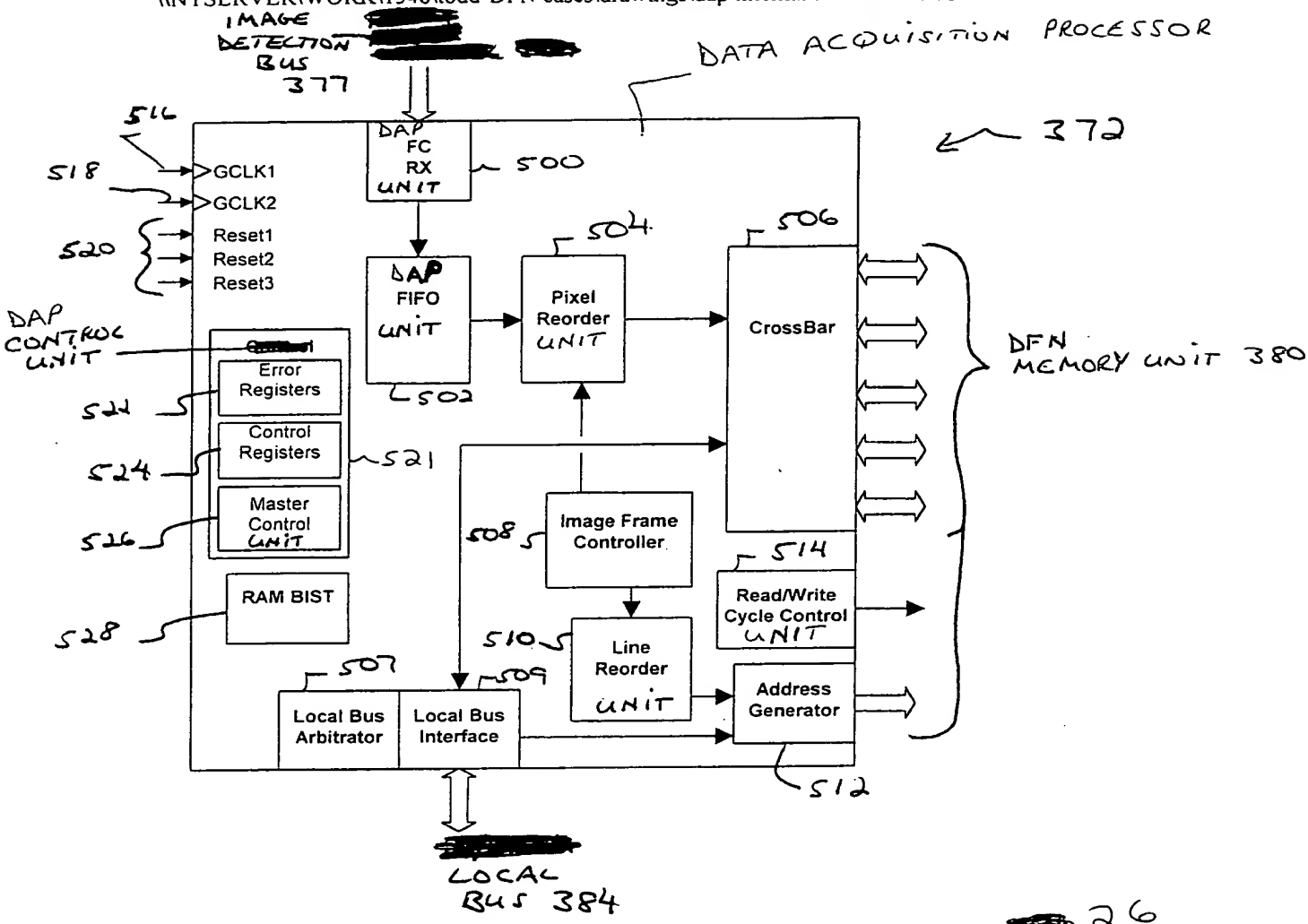


FIG. [redacted] 26

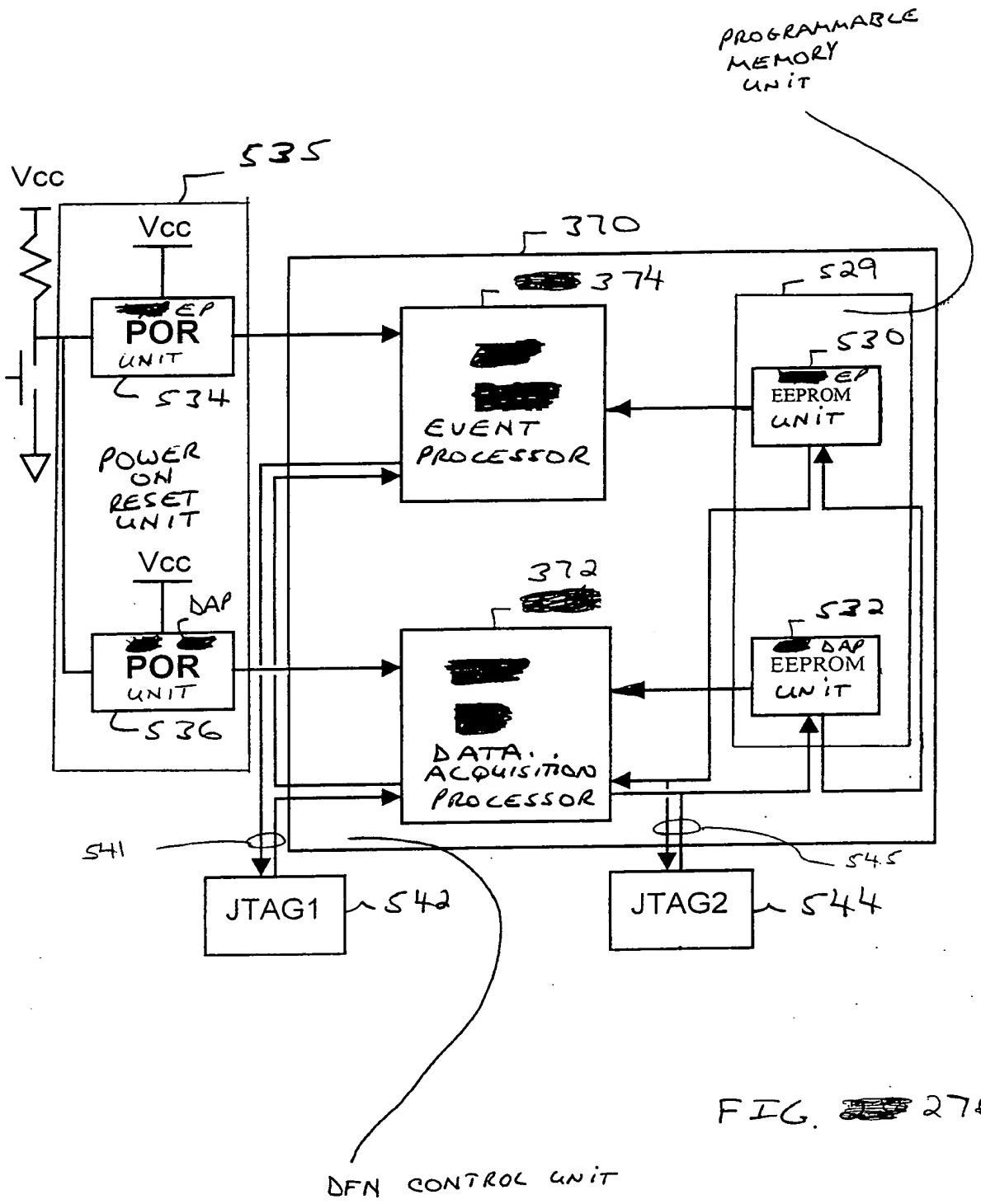

PROGRAMMABLE MEMORY UNIT
535
Vcc
Vcc
370
374
529
EP
POR
UNIT
534
530
EP
EEPROM
UNIT
EVENT PROCESSOR
POWER ON RESET UNIT
Vcc
372
DAP
532
DAP
POR
UNIT
536
DAP
EEPROM
UNIT
DATA ACQUISITION PROCESSOR
541
545
JTAG1
542
JTAG2
544
DFN CONTROL UNIT

FIG. 27

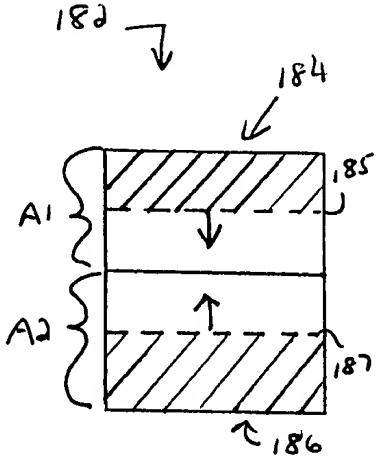


FIG. ~~28A~~
28

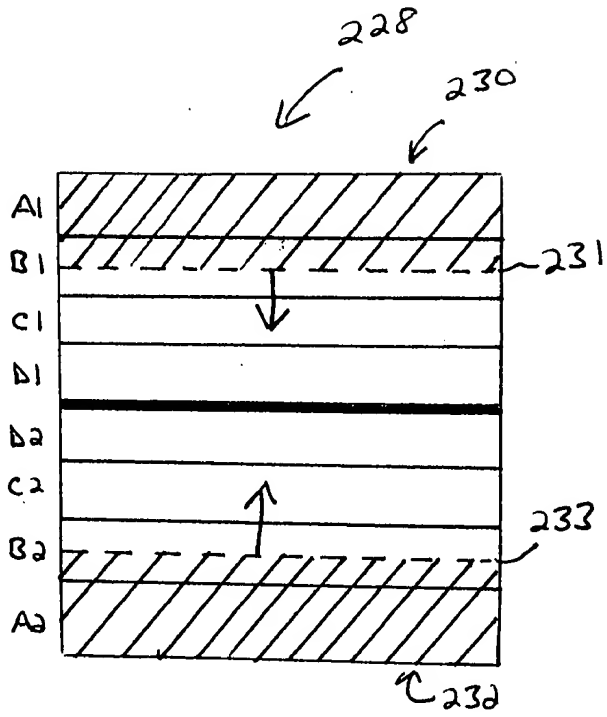


FIG. ~~28B~~
29

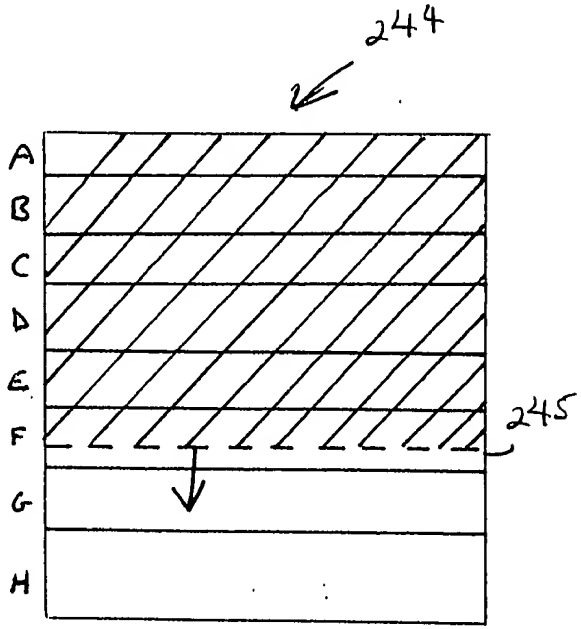


FIG. ~~28C~~
30

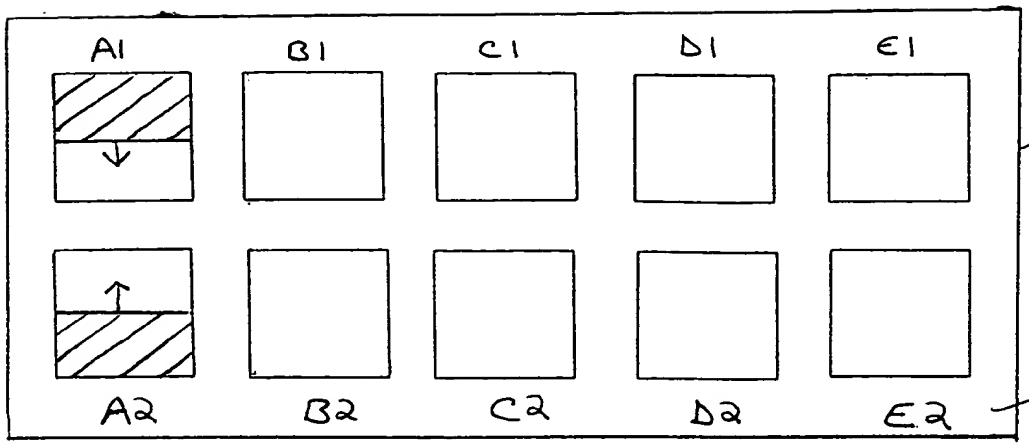


FIG. ~~19A~~ 31

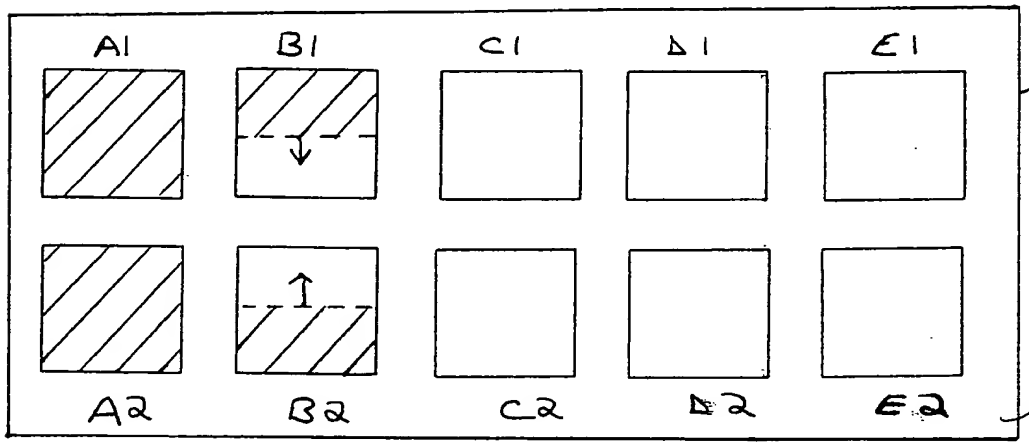


FIG. ~~19B~~ 32

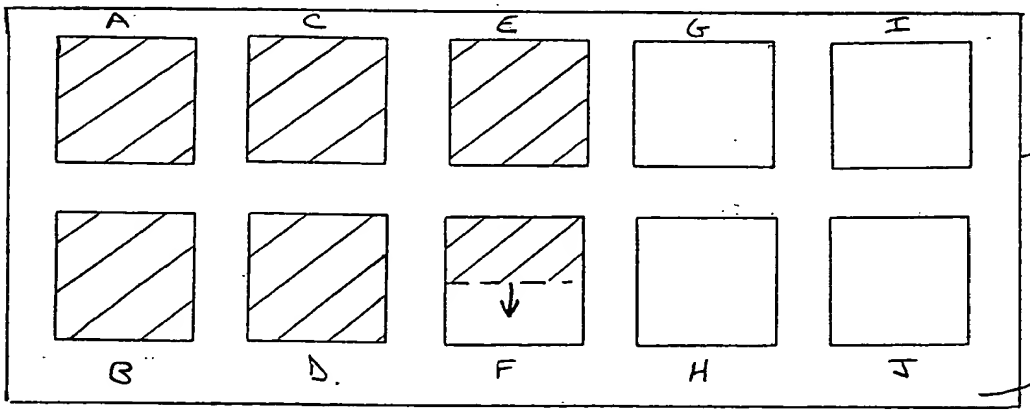


FIG. ~~19C~~ 33

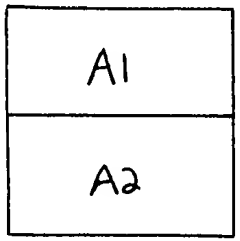


FIG. ~~3A~~ 34

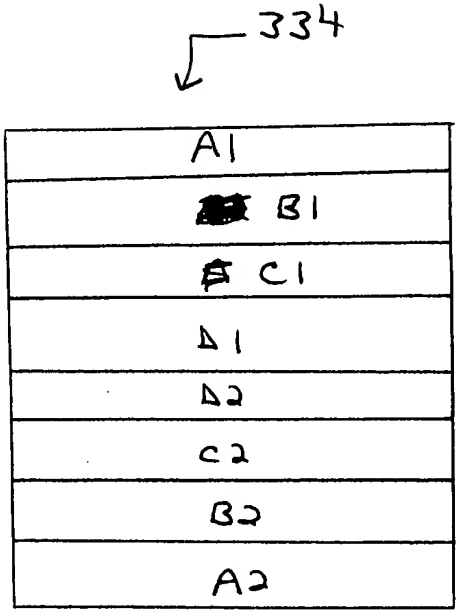


FIG. ~~3B~~ 35

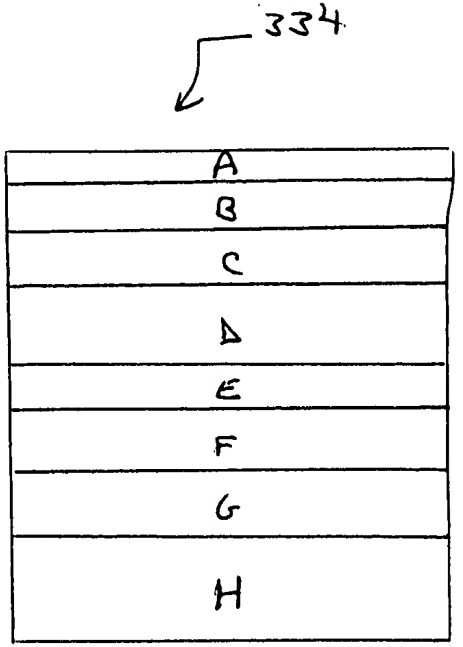


FIG. ~~3C~~ 36

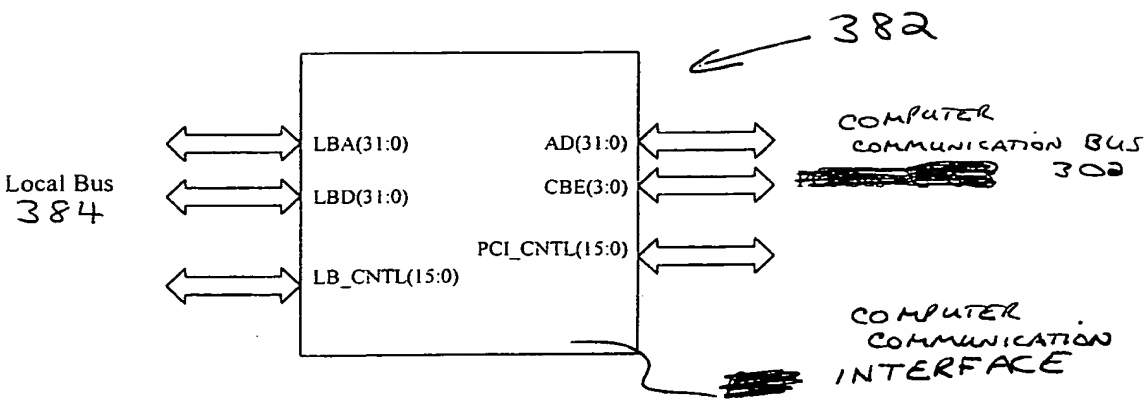


FIG. [redacted] 37

W:\1346\todd-DFN cases\drawings\fibre channel system.doc

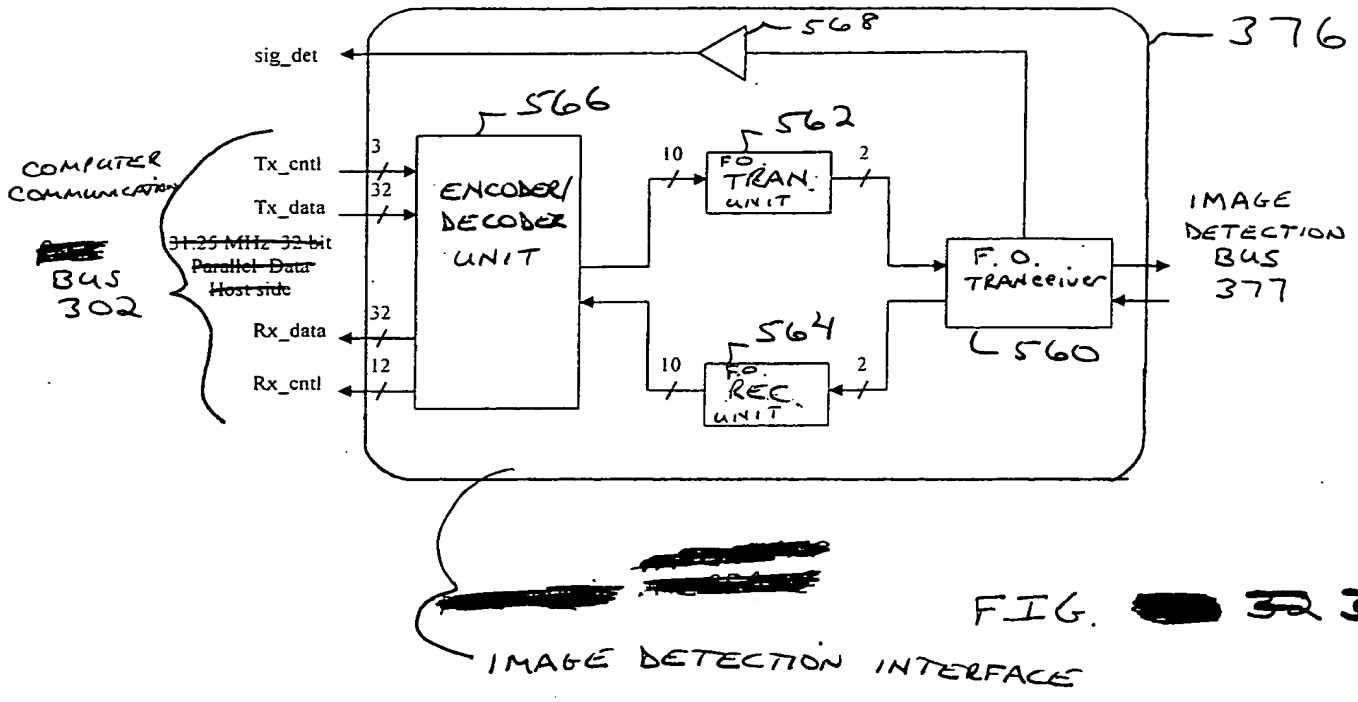


FIG. [redacted] 38

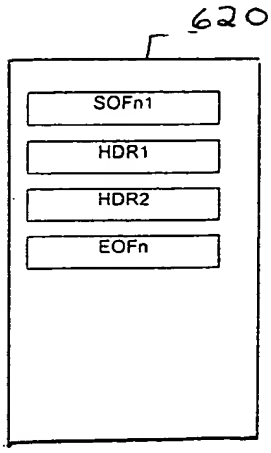


FIG. [redacted] 39

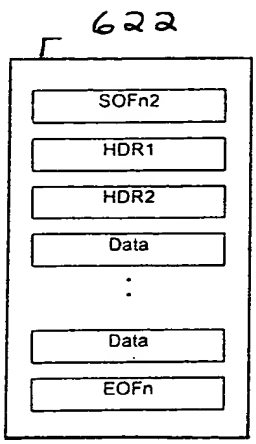


FIG. [redacted] 40

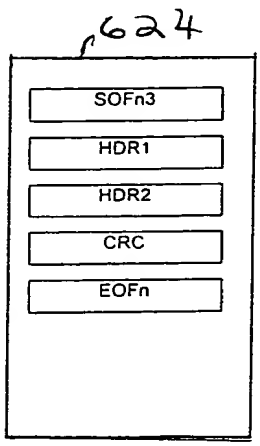


FIG. [redacted] 41

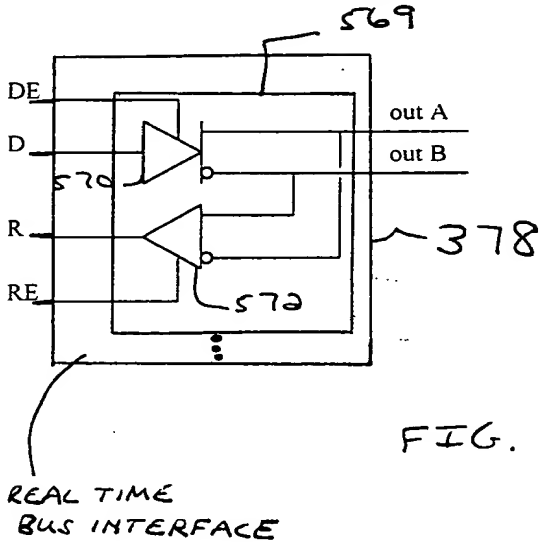


FIG. [redacted] 42

W:\1346\todd-DFN cases\drawings\clock distribution.doc

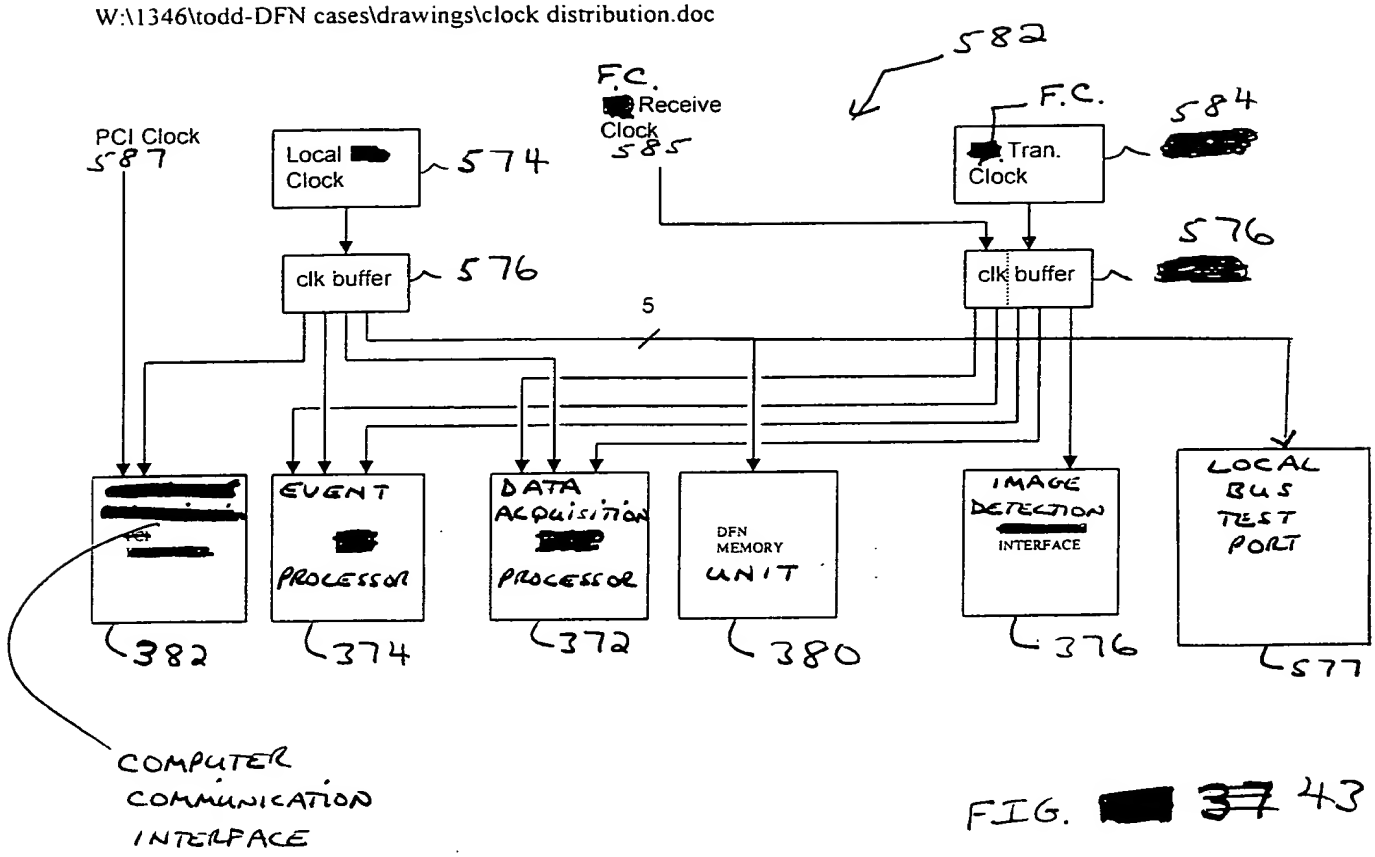
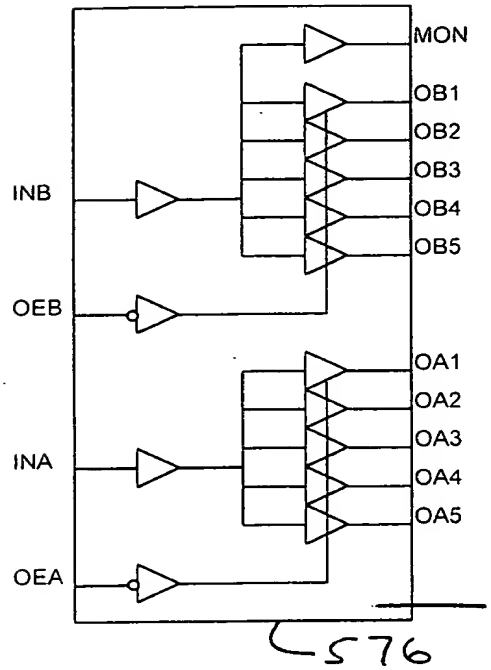


FIG. [redacted] 37 43

W:\1346\todd-DFN cases\drawings\clock buffer chip.doc



CLOCK BUFFER

FIG. 44

W:\1346\todd-DFN cases\drawings\reset distribution.doc

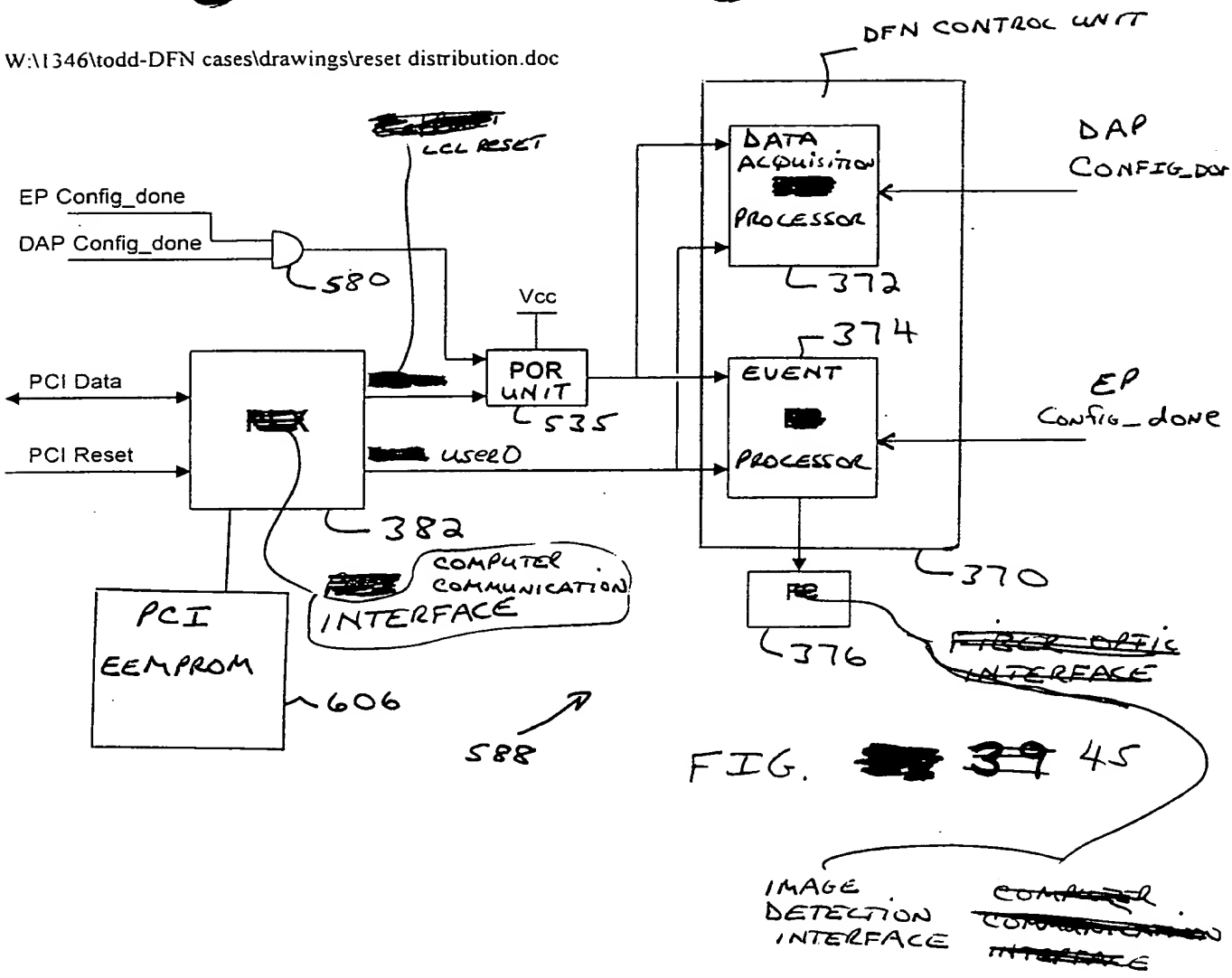
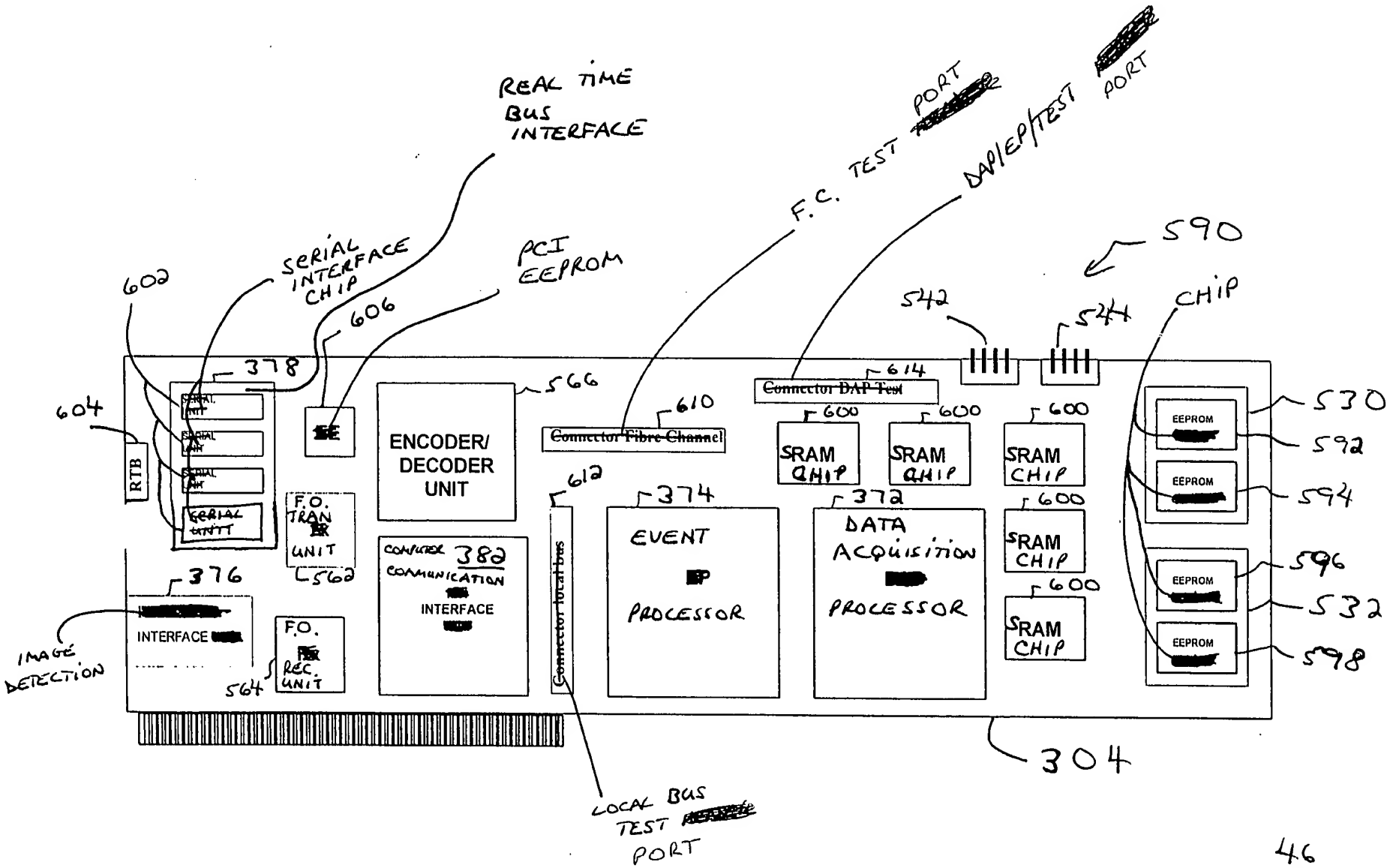


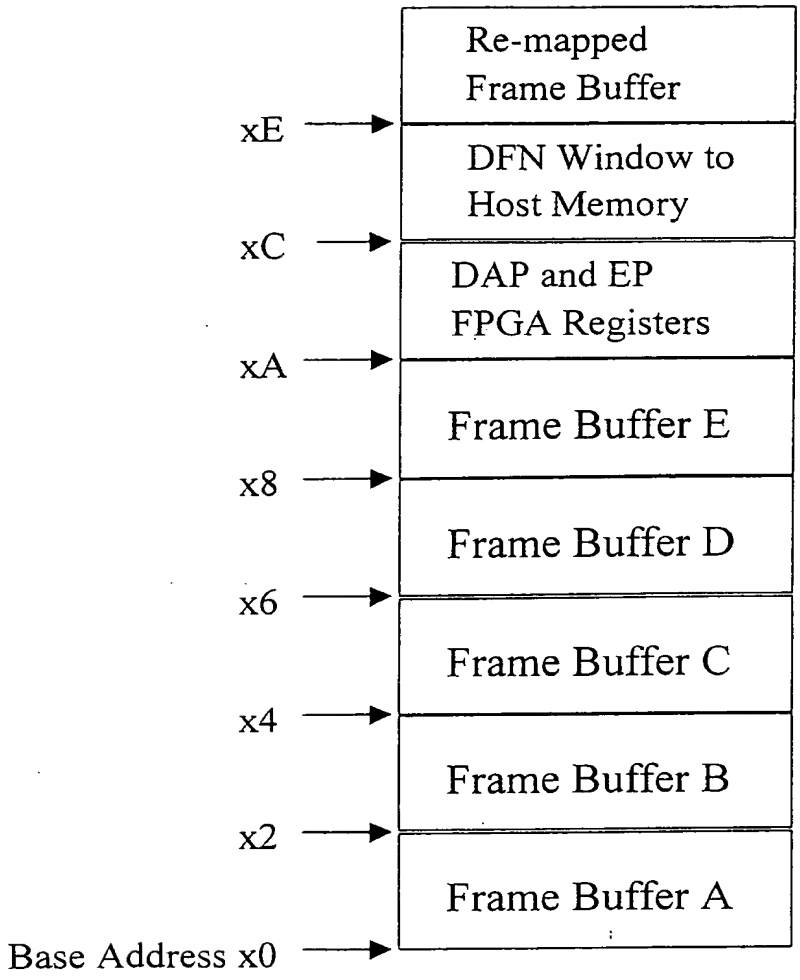
FIG. [redacted] 39 45


REAL TIME BUS INTERFACE
F.C. TEST PORT
DAP/EP/TEST PORT
590
602
SERIAL INTERFACE CHIP
606
PCI EEPROM
542
544
CHIP
604
378
566
614
610
600
530
592
594
596
532
598
RTB
ENCODER/ DECODER UNIT
Connector DAP Test
Connector Fibre Channel
SRAM CHIP
EEPROM
F.O. TRAN UNIT
562
612
374
372
376
380
COMPUTER COMMUNICATION INTERFACE
EVENT PROCESSOR
DATA ACQUISITION PROCESSOR
Connector local bus
IMAGE DETECTION
564
F.O. REC. UNIT
304
LOCAL BUS TEST PORT

46

FIG.

W:\1346\todd-DFN cases\drawings\FIG. 41.doc



Mapping of 16 MByte PCI Address Space

FIG. 47

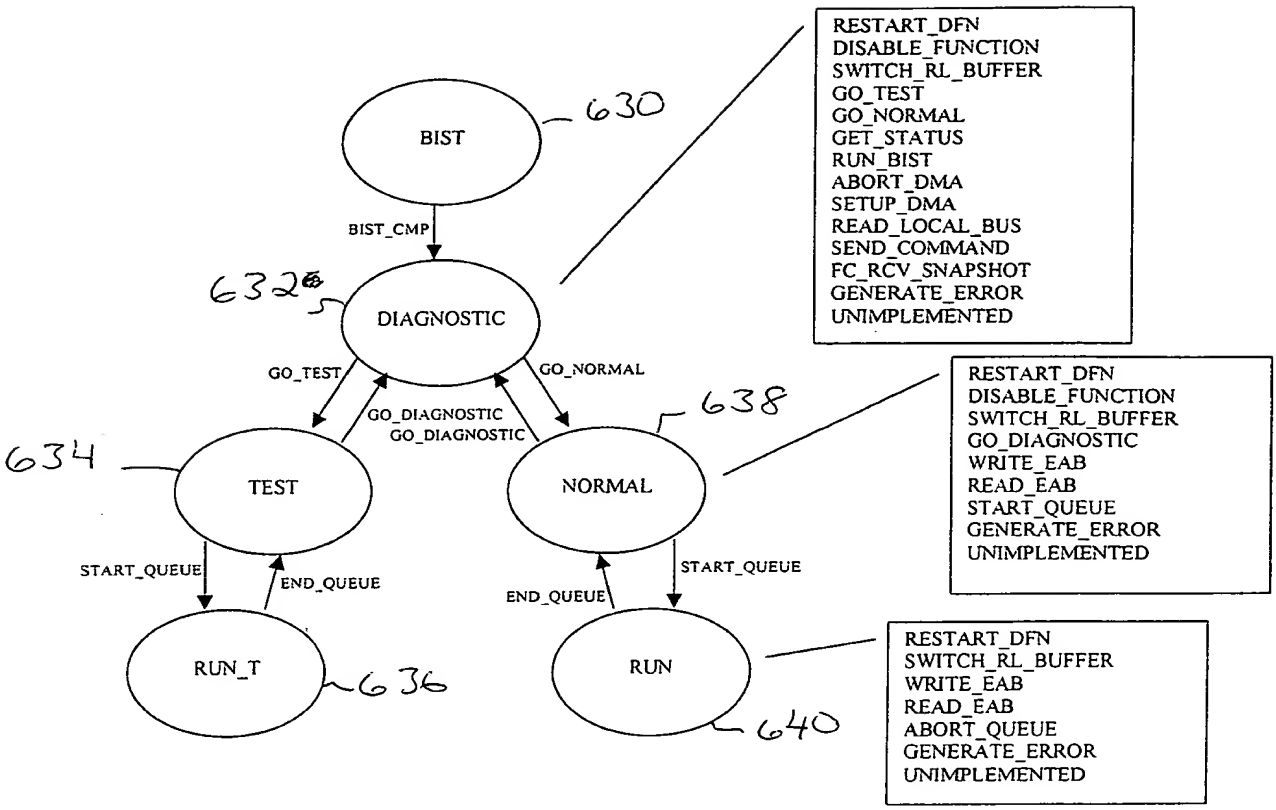

BIST
630
BIST_CMP
DIAGNOSTIC
632
GO_TEST
GO_NORMAL
GO_DIAGNOSTIC
GO_DIAGNOSTIC
TEST
634
NORMAL
638
START_QUEUE
END_QUEUE
START_QUEUE
END_QUEUE
RUN_T
636
RUN
640
RESTART_DFN
DISABLE_FUNCTION
SWITCH_RL_BUFFER
GO_TEST
GO_NORMAL
GET_STATUS
RUN_BIST
ABORT_DMA
SETUP_DMA
READ_LOCAL_BUS
SEND_COMMAND
FC_RCV_SNAPSHOT
GENERATE_ERROR
UNIMPLEMENTED
RESTART_DFN
DISABLE_FUNCTION
SWITCH_RL_BUFFER
GO_DIAGNOSTIC
WRITE_EAB
READ_EAB
START_QUEUE
GENERATE_ERROR
UNIMPLEMENTED
RESTART_DFN
SWITCH_RL_BUFFER
WRITE_EAB
READ_EAB
ABORT_QUEUE
GENERATE_ERROR
UNIMPLEMENTED

FIG. 48

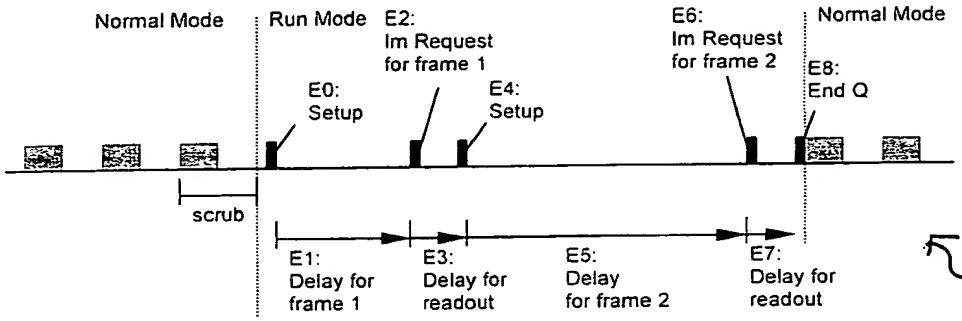


FIG. 49

Event Mnemonic	Event (showing size of arguments)	Op Code (hex)	Data (bytes)	Total (bytes)
Endq	Endq	14	0	1
Delay (T)	Delay (0xff ff ff ff)	10	4	5
Send (command, value)	Send (0xff ff ff ff, 0xff ff ff ff)	04	8	9
LoopKN (K, N)	LoopKN (0xff ff, 0xff)	0C	3	4
LoopKF (K, F)	LoopKF (0xff ff, 0xff ff ff)	0D	5	6
Wait (F)	Wait (0xff ff ff)	09	3	4
Flag (F)	Flag (0xff ff ff)	08	3	4

FIG. 50

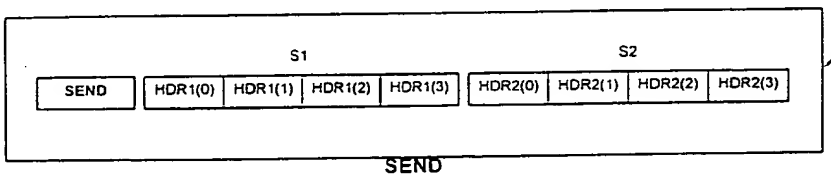


FIG. 51

Error Mnemonic	Description of Error
FC_TIMEOUT	Timeout expired with no ACK detected
FC_BAD_ACK	ACK did not match transmitted command
FC_EXTRA_ACK	Unexpected ACK received
FC_EXTRA_CMD	New Send event while waiting for ACK from previous Send
SIG_DETN	No input signal power on Fibre Channel (cable disconnected?)
RXERROR	Fibre Channel receiver detected bad data (defective chipset?)
WRDSYNCN	Fibre Channel Data link unsynchronized
CRXS(1)	Bad Received CRC detected (Fiber-optic cable problem?)
CRXS(3) and CRXS(2)	Bad order in link state machine (defective chipset?)

672

FIG. [redacted] 52

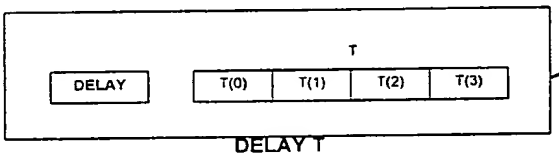


FIG. [redacted] 53

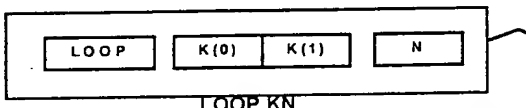


FIG. [redacted] 54

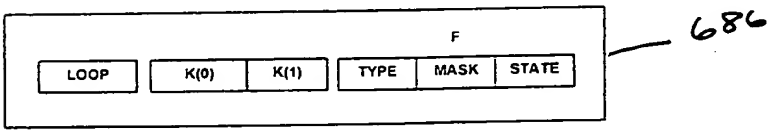


FIG. [redacted] 55

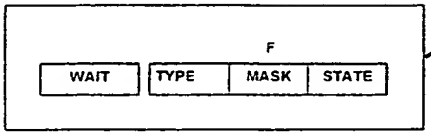


FIG. [redacted] 56

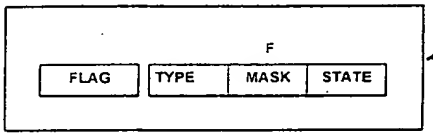


FIG. [redacted] 57

FIG. [redacted] 58

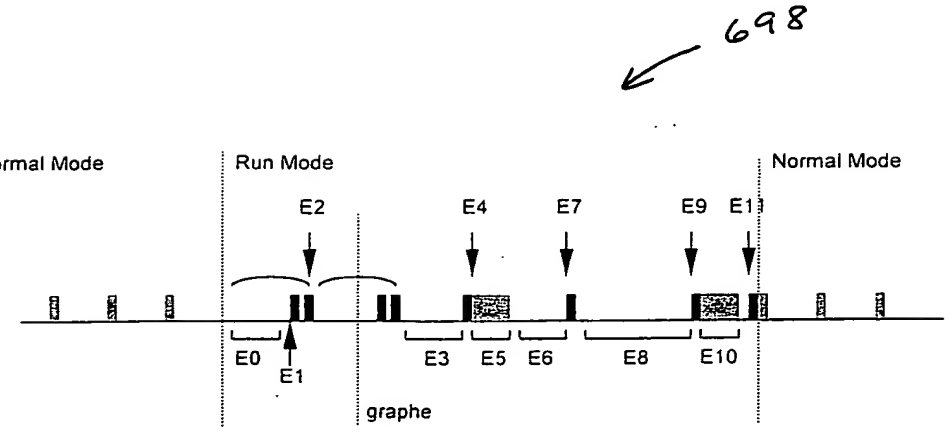


FIG. [redacted] 59

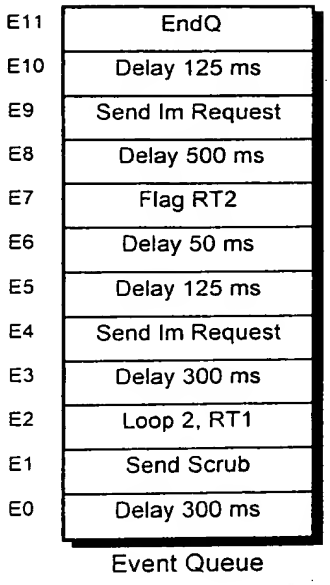

E11
EndQ
E10
Delay 125 ms
E9
Send Im Request
E8
Delay 500 ms
E7
Flag RT2
E6
Delay 50 ms
E5
Delay 125 ms
E4
Send Im Request
E3
Delay 300 ms
E2
Loop 2, RT1
E1
Send Scrub
E0
Delay 300 ms
Event Queue
700

FIG. 60

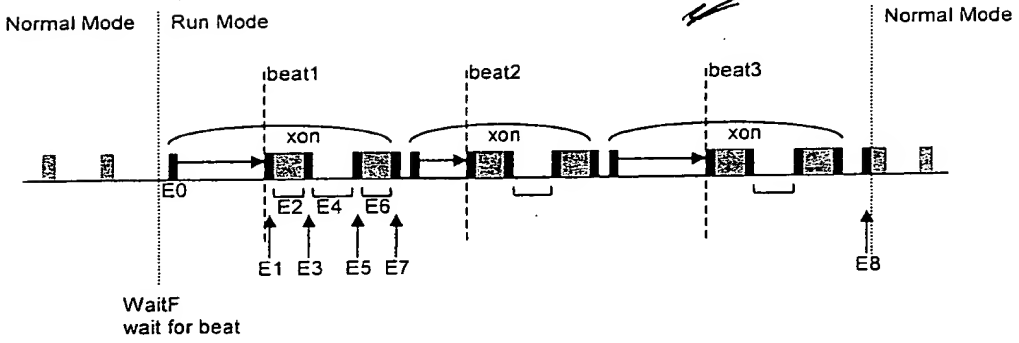

702
Normal Mode
Run Mode
Normal Mode
beat1
beat2
beat3
xon
xon
xon
E0
E2
E4
E6
E1
E3
E5
E7
E8
WaitF
wait for beat

FIG. 61

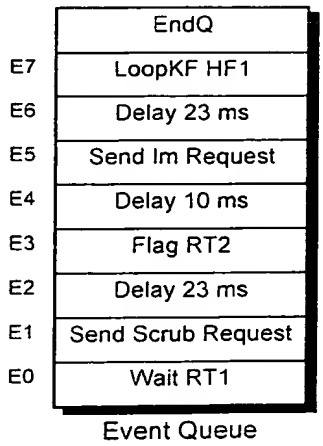

EndQ
E7
LoopKF HF1
E6
Delay 23 ms
E5
Send Im Request
E4
Delay 10 ms
E3
Flag RT2
E2
Delay 23 ms
E1
Send Scrub Request
E0
Wait RT1
Event Queue
704

FIG. 62

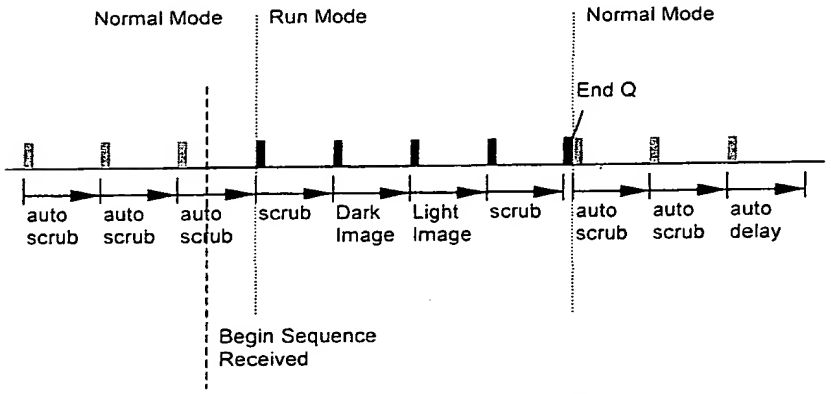

Normal Mode
Run Mode
Normal Mode
End Q
auto scrub
auto scrub
auto scrub
scrub
Dark Image
Light Image
scrub
auto scrub
auto scrub
auto delay
Begin Sequence Received

FIG. 63

```
sequence_begin ();

# define qv defaults:
%qv1 =('delay_qv' => 5000);

# call frame with qv's
frame_type1 (NULL, \%qv1, 1);

sequence_end ();
```

FIG. 64

```
sub frame
{
  $QVf = 'frame';

  %qv = ('delay_qv'  => [10000]);
  %qp = ();

  compile_init(@_,\%qp,\%qv,$QVf);

    Delay('delay_qv');

  compile_finit();
}
```

FIG. 65

```
pDFN->DFNChangeQueueVariable
  (
   (char *)SymName,      // variable name
   (char *)sndBuf,       // new value
   BufSize,              // num bytes to write
   (ULONG *)&debug       // developer info
    );
```

FIG. 66

User Application

```
// load and run the event sequence
pDFN->DFNBeginSequenceNoMappingNoLog
    (snum,"d:\\HF.bin");

//assign data to be passed
sndBuf = 25000;

// change the queue variable
pDFN->DFNChangeQueueVariable
 (
  (char *)SymName,       // variable name
  (char *)sndBuf,        // new value
  (ULONG)sizeof sndBuf,  // num bytes to write
  (ULONG *)&debug        // developer info
   );
```

FIG. 67

Perl Script

```
sub frame_type1
{
  $HFfrm = 'frame_type1';

  %qv = ('delay_qv'  => [20000] );
  %qp = ();

  $image_cmd   = [0x800000,0x0];

 compile_init(@_,\%qp,\%qv,$HFfrm);

   Send($image_cmd);
   Delay('delay_qv');
   LoopKF(2,0xAAFF01);

 compile_finit();
}
```

FIG. 68

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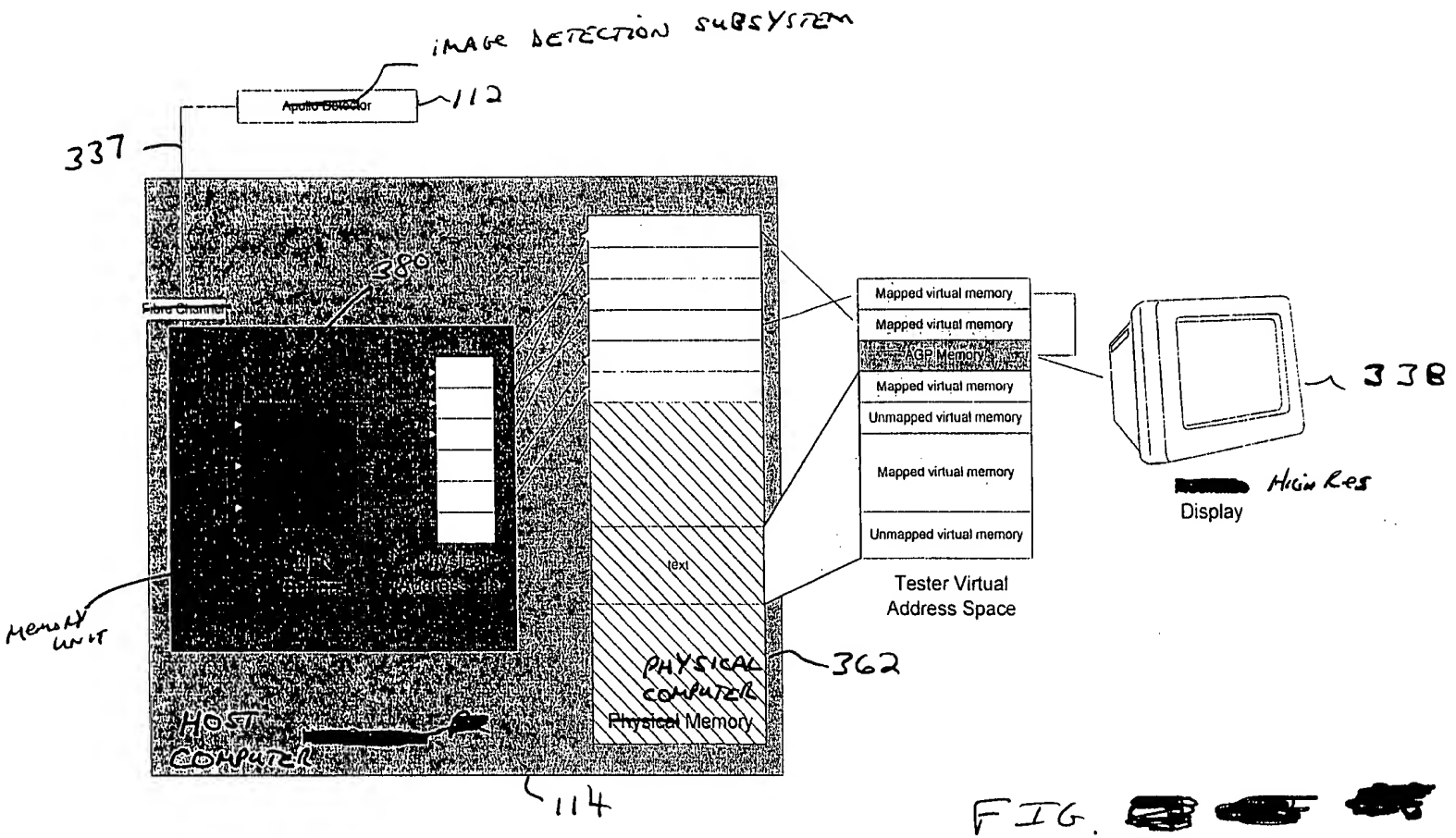
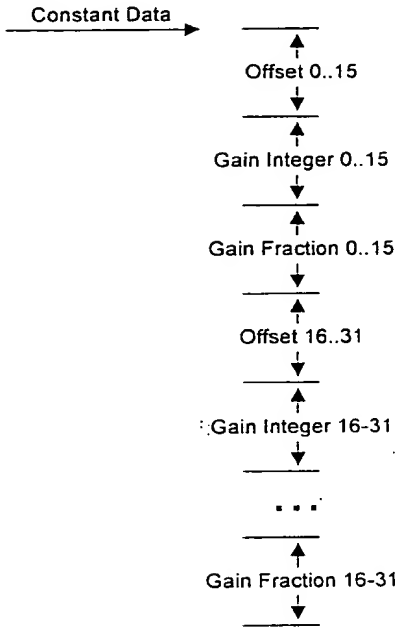


FIG. [redacted] 69

\\NTSERVER\WORK\1346\todd-DFN cases\drawings\Constant Memory Format.doc

44



Constant Memory Format

FIG. [redacted]

70

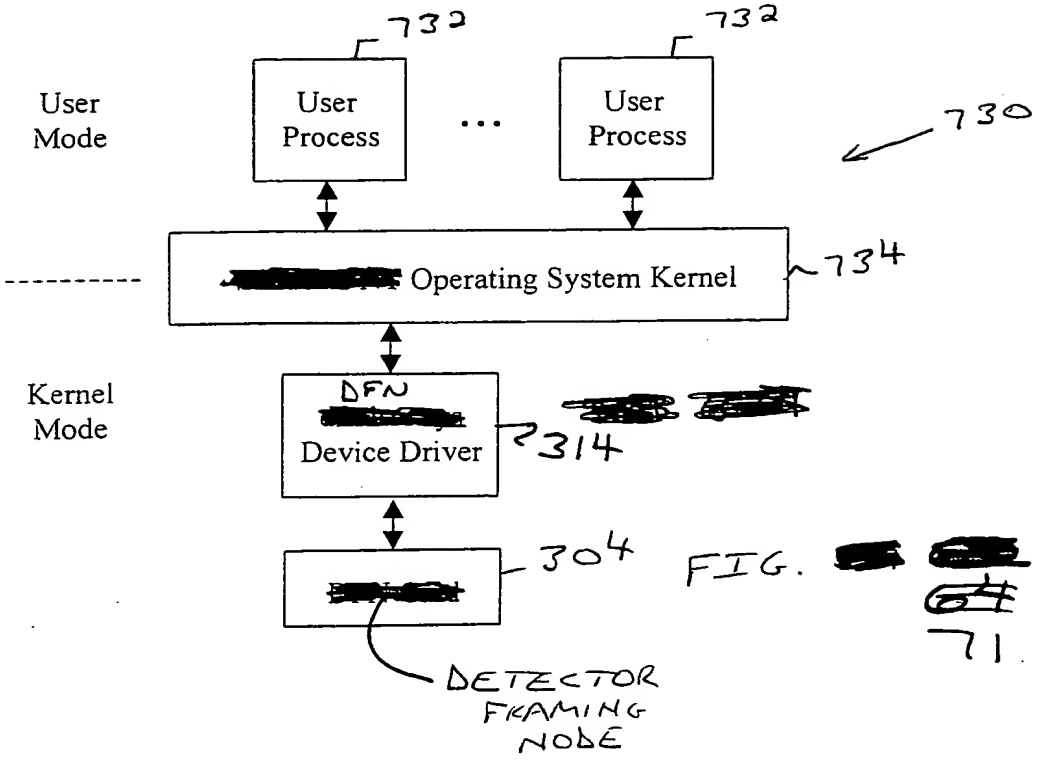

User Mode
User Process
User Process
732
732
730
Operating System Kernel
734
Kernel Mode
DFN
Device Driver
314
304
DETECTOR FRAMING NODE

FIG. 71

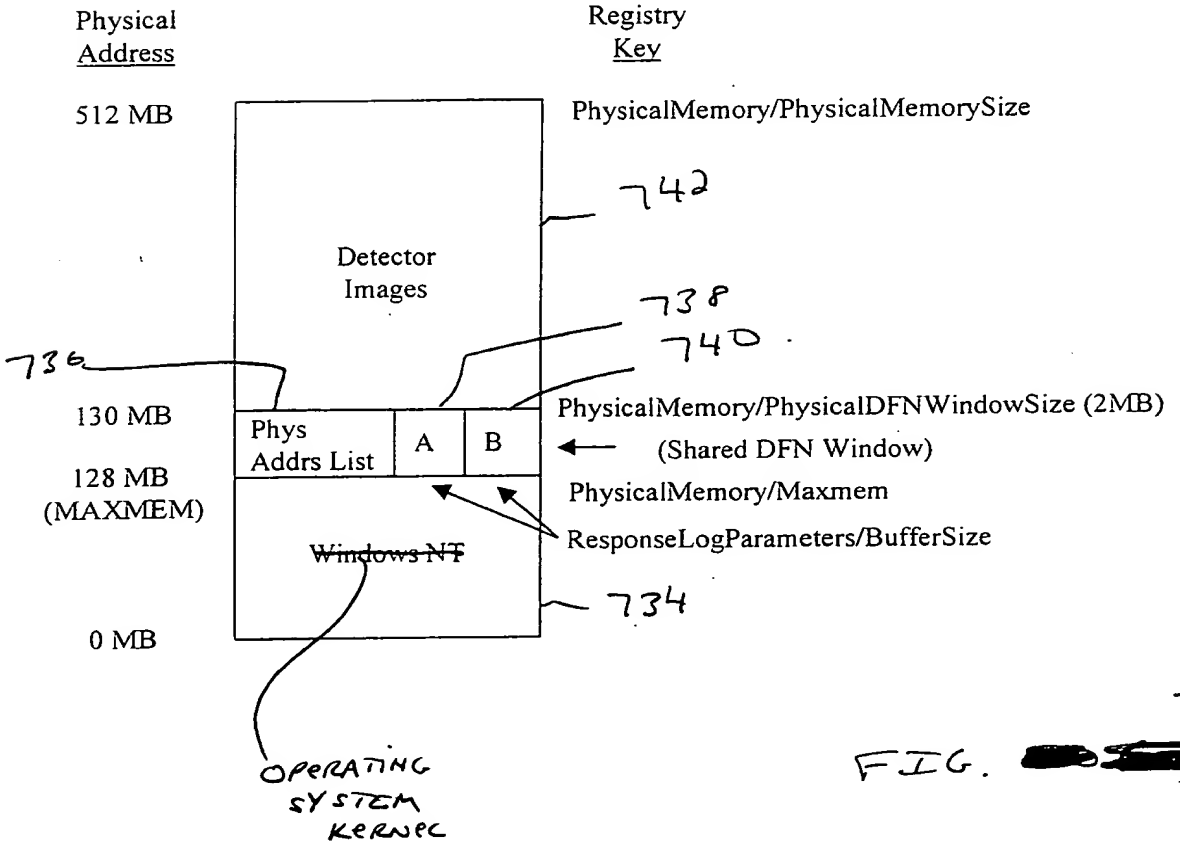

Physical Address
Registry Key
512 MB
PhysicalMemory/PhysicalMemorySize
742
Detector Images
738
740
736
130 MB
Phys Addrs List
A
B
PhysicalMemory/PhysicalDFNWindowSize (2MB)
(Shared DFN Window)
128 MB (MAXMEM)
PhysicalMemory/Maxmem
ResponseLogParameters/BufferSize
Windows NT
734
0 MB
OPERATING SYSTEM KERNEL

FIG. 72

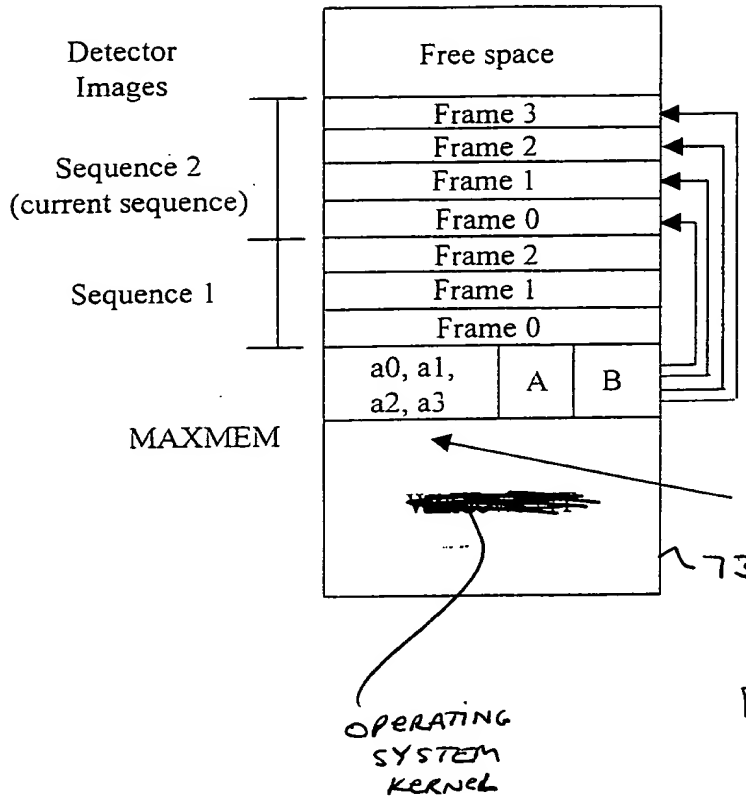


FIG. [redacted] 73